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IBM®

Maintenance Library

3830 Storage Control, Model 2

This Volume

Volume 1	Volume 2	Volume 3
PLAN MLM LAYOUT	OLT DIAG	PWR POWER
LGND LEGEND ABBREVIATIONS	SENSE DATA	INTR ODUCTION
MLX CROSS REFERENCE	FSI FAULT SYSTEM INDEX	CMD COMMANDS
START MAINT	CTRL CONTROL	MIC ROPROGRAM
MSG SYSTEM MESSAGES	MPL 23FD	MICFL DIAG FLOW
PANEL	MPL ATTACHMENT	LOC ATIONS
MICRO DIAG-NOSTICS	CHL-I CHANNEL INTERFACE	INST ALLATION
	CTL-I CONTROL INTERFACE	INDEX

3830-2

AA0200 Seq 1 of 2	2346970 Part Number	437402A 15 Mar 72	437405 15 Aug 72	437408 16 Oct 72	437414 4 Jun 73			

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PREFACE

The 3830-2 Maintenance Library is designed to assist the Customer Engineer in achieving a repair when a failure is discovered either by a customer who has placed a call, or by the CE performing system checkout or routine EREP analysis. The manual assumes that the majority of calls can be handled by a product-trained CE with help available from a support-trained CE when needed. Maintenance material is given prominence in the manual organization, with emphasis on "how to fix" rather than on theory of operation.

Information pertaining to MST component circuits, ALD's, and FEALD's will be found in the IBM Maintenance Library, *Logic Blocks Automated Logic Diagrams SLT, SLD, ASLT, MST,* Order No. SY22-2798.

Information pertaining to MST packaging, tools, and wiring change procedure will be found in the FE Theory of Operation, *IBM Monolithic System Technology,* Order No. SY22-6739.

Information pertaining to MST power supplies and components will be found in the FE Theory of Operation, *IBM Power Supplies,* Order No. SY22-2799.

MAINTENANCE LIBRARY ORDERING PROCEDURE (IBM INTERNAL)

Individual pages of the 3830-2 Maintenance Library can be ordered from the San Jose plant by using the *Wiring Diagram/ Logic Page Request* (Order No. 120-1679). Indicate machine type (3830-2) and, in the columns headed "Logic Page", enter the sequence number, part number, and EC number. Groups of pages can be ordered by including a description (section, volume, etc.) and the machine serial number.

CE-MLM Feedback forms are provided at the front of this volume for reader comments. If the forms have been removed, send your comments to the address below.

This manual was prepared by the IBM General Products Division, Product Publications, Department G24, San Jose, California 95193.

SAFETY

Be constantly aware of hazardous situations when working on the 3830-2 Storage Control. Take time to review the CE safety practices listed below which have been reprinted from the pocket-size card available from Mechanicsburg (Order No. S229-1264).

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it; for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment - eliminate unsafe acts.

ARTIFICIAL RESPIRATION

General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects. Pull tongue forward.
3. Loosen Clothing – Keep Victim Warm
   Take care of these items after victim is breathing by himself or when help is available.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

1. Place victim on his back immediately.
2. Clear throat of water, food, or foreign matter.
3. Tilt head back to open air passage.
4. Lift jaw up to keep tongue out of air passage.
5. Pinch nostrils to prevent air leakage when you blow.
6. Blow until you see chest rise.
7. Remove your lips and allow lungs to empty.
8. Listen for snoring and gurglings – signs of throat obstruction.
9. Repeat mouth to mouth breathing 10-20 times a minute. Continue rescue breathing until victim breathes for himself.

Thumb and finger positions

Final mouth-to-mouth position

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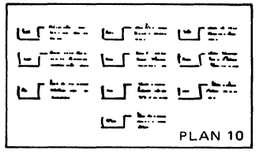
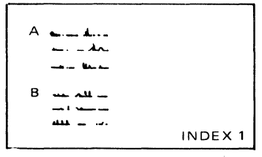
IBM 3830-2 MAINTENANCE LIBRARY

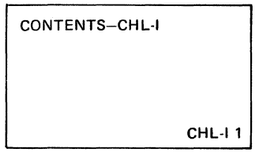
HOW TO FIND INFORMATION:



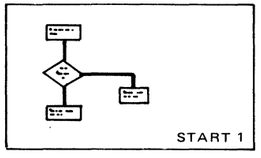
DOCUMENTATION PLAN (PLAN 10) defines major sections of the manual. Where practical, documentation is arranged in sections corresponding to the natural breakdown of machine elements.



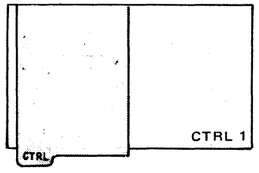
A SUBJECT INDEX gives access to specific subjects.



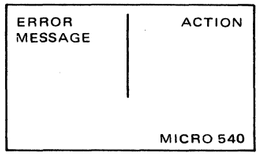
FIRST PAGE OF EACH SECTION indicates the contents of the section and may contain other pertinent information.



START is the starting point for all maintenance. This section is designed to get you quickly on the right track and either lead you to a solution or direct you to more specialized information elsewhere in the manual.

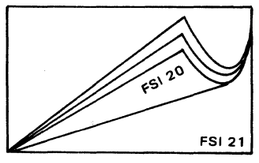


DIVIDER TABS provide rapid accessibility and allow efficient cross referencing between and within maintenance library sections.

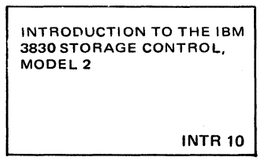


ERROR DICTIONARIES (MICRO and OLTS) reference appropriate maintenance procedures for microdiagnostic and online—test error messages.

FAULT SYMPTOM INDEX (FSI) references appropriate maintenance procedures for errors identified by sense data.



PAGE NUMBERS in "thumbing" position may be rapidly scanned by flipping pages.



WANT TO LEARN THE 3830-2? The INTR, CMD, and MIC sections contain instructional and recall material that is useful either for initial training or as backup information during the maintenance activity.

3830-2

AA0300	2346971
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437402A	437403	437404	437405	437408	437414	
15 Mar 72	21 Apr 72	23 Jun 72	15 Aug 72	16 Oct 72	4 Jun 73	

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MAINTENANCE LIBRARY DOCUMENTATION PLAN

VOLUME 1

PLAN — The documentation plan defines organization of manual and content of major manual sections.

LGND — Legend pages contain descriptions of symbols, conventions, and abbreviations used in the MLM.

MLX — Maintenance Library Cross Reference (MLX) pages provide an index of entry/exit lines in this MLM and in MLMs of units that interface with the 3830-2.

START — The starting point for all maintenance activity. High level diagnostic MAPs help isolate the fault to a single conceptual unit. A preventive maintenance schedule is included.

MSG — Performance data collection and analysis. Includes descriptions and example of statistical data, error data, and environmental data.

PANEL — Description and operation of the 3830-2 CE panel. Includes error collection and analysis from CE panel.

MICRO — MICRO diagnostics operating summary and error message dictionary.

VOLUME 2

OLT — Online tests (OLTs) operating summary and error message dictionary.

SENSE — Detailed description of sense information.

FSI — Fault Symptom Index (FSI) used with error code derived from sense data.

CTRL — The control (CTRL) unit is the heart of the 3830-2 Storage Control. Detailed MAPs are provided for trouble diagnosis. Backup information includes descriptions of the control storage, microprogram instruction decode, general purpose registers, and arithmetic logic unit (ALU).

MPL23FD — Theory and maintenance information for the microprogram load (MPL) file.

MPLATTACHMENT — Detailed MAPs followed by descriptions of MPL file/3830-2 attachment circuits and initial microprogram load (IMPL).

CHL-I — Detailed MAPs and descriptive information for the channel interface conceptual unit, including the *Two Channel Switch* feature and *Two Channel Switch, Additional* feature.

CTL-I — Explains how the control interface allows selection and control of a disk drive.

VOLUME 3

PWR — Detailed MAPs of the 3830-2 power system. Includes sequencing and distribution diagrams.

INTR — Introduction to IBM 3830 Storage Control, Model 2. Describes the various conceptual units which make up the 3830-2. Shows data and control flow within and between the 3830-2 and the disk storage modules.

CMD — Microprogram and hardware operations for the various commands and operations performed by the disk storage subsystem.

MIC — Microprogram information needed to read CLDs. Describes the micro-block format, the various microword formats, and register assignments. Also included are microprogram instruction examples.

MICFL — Microdiagnostic descriptions and flowcharts of tests to aid in trouble analysis.

LOCATIONS — Structural and component locations for the 3830 Storage Control, Model 2.

INSTALLATION — Installation instructions for the IBM 3830-2.

INDEX — Alphabetical subject index of maintenance library.

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- Logic Block Special Symbols
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- Logic Diagrams
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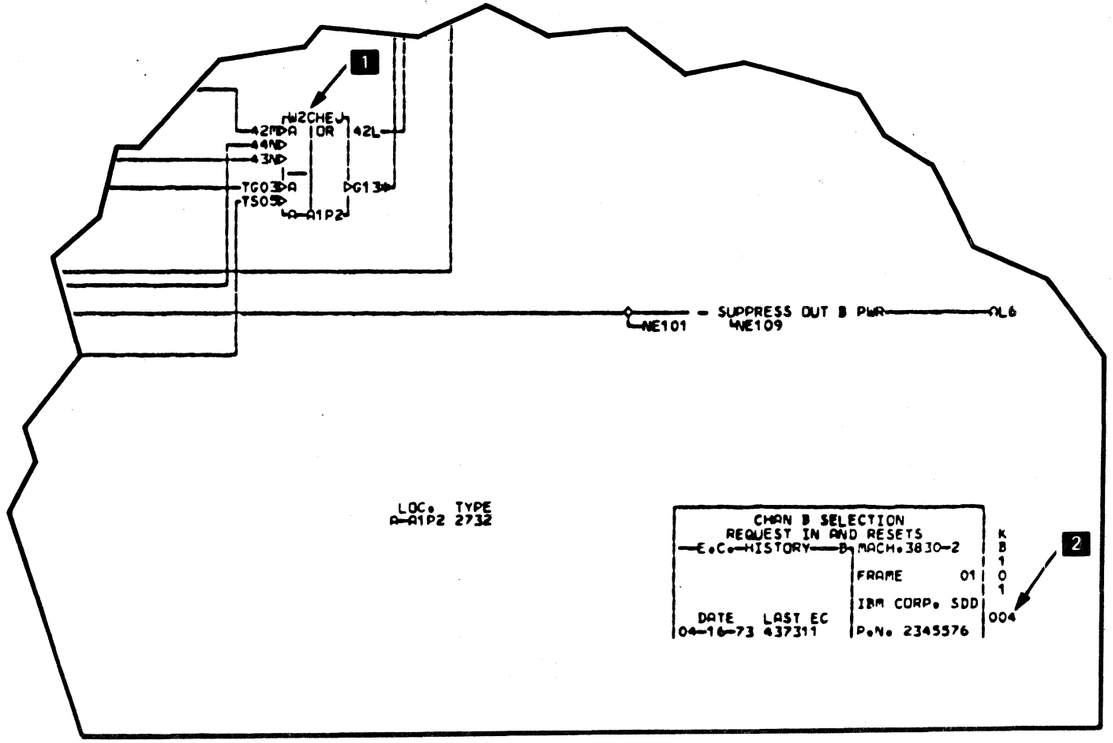
ALD VERSION INFORMATION

3830-2 ADDITIVE CARD CODES

1
- W2CH = Two Channel Switch
- W4CH = Two Channel Switch, Additional

3830-2 MACHINE VERSION CODES

2
- 000 = Basic
- 001 = Extended Control Store
- 002 = String Switch Attachment
- 004 = Two Channel Switch Additional without String Switch Attachment



LEGEND (Part 1 of 6)

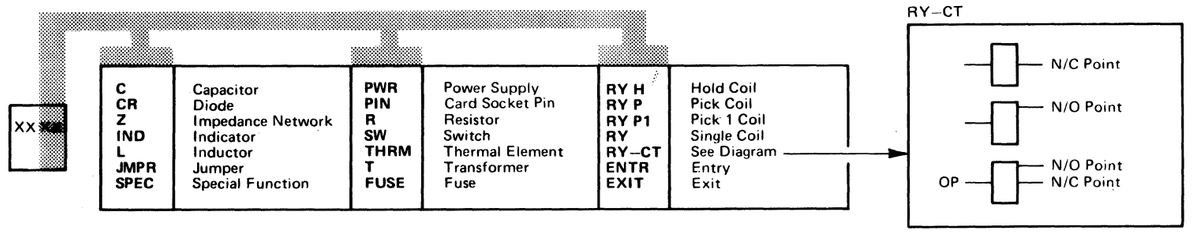
Logic Diagrams

In the following logic representation, line signal levels are disregarded. The purpose of the symbols and descriptions is to provide a reference for servicing. Additional information can be found in IBM Maintenance Library, *Logic Blocks, Automated Logic Diagrams SLT, SLD, ASLT, MST,* Order No. SY22-2798; and IBM Maintenance Library, *Monolithic System Technology, Theory of Operation, Packaging, Tools and Wiring Change Procedure,* Order No. SY22-6739.

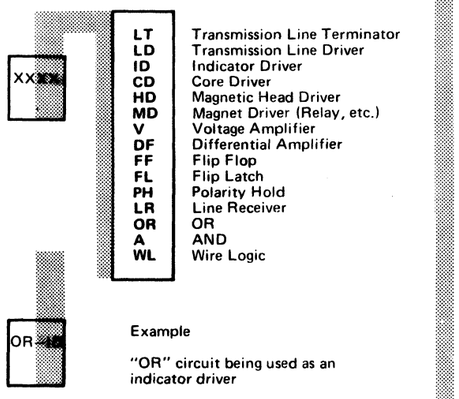
Function Blocks

- A — **AND**
- OR — **OR**
- OE — **Exclusive Or** Output is active if either input, but not both, is active.
- EV — **Even** An even number of inputs (including zero) must be active to produce an active output.
- OD — **Odd** An odd number of inputs must be active to produce an active output.
- LIM — **Limiter** Limits one or both extremes of a wave form.
- (time) SS — **Single Shot**
- ST — **Schmitt Trigger**
- (time) TD — **Time Delay**
- PG — **Pulse Generator**
- (frequency) OSC — **Oscillator**
- D — **Driver**
- AR — **Amplifier**
- A-(N) — **Threshold**
- CV — **Signal Mode Converter**
- Z — **Impedance Network**
- N — **Negator** Inverts logic
- SUM — **Algebraic Sum**
- CS — **Current Switch**
- (type) FLTR — **Filter**

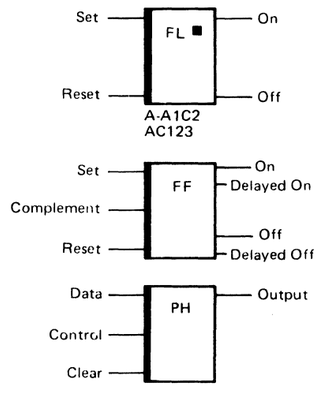
Logic Block Special Symbols



Logic Block Suffixes



Storage Elements



Flip-Latch
Symbol (■) identifies indicator lamp. Card location and ALD (logic) page reference at bottom of block.

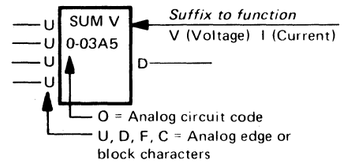
Flip-Flop
Shift input is shown by a P (shift to active) or N (shift to inactive). Delayed output (D) does not change state until end of shift pulse.

Polarity Hold
Output becomes active when data line and control line are both made active. Output remains active when control line becomes inactive. PH registers can have contents changed by strobing new data in with the control line; reset is unnecessary.

Analog/Digital Logic Blocks

Digital Logic: Conveys information by a device assuming a limited number of discrete states, usually two.

Analog Logic: Conveys information through signals that vary in amplitude, frequency, phase, or compound frequency throughout a continuous operating range or time period.



U (Up): A voltage or current mode signal that performs its function as the voltage changes toward positive or as the magnitude of the current increases.

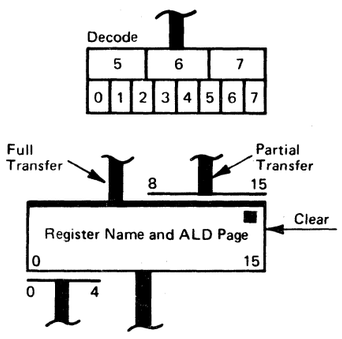
D (Down): A voltage or current mode signal that performs its function as the voltage changes toward negative or as the magnitude of the current decreases.

U-D: As shown in example, indicates signal inversion.

F (Frequency): A signal that conveys information by the combined effect of many individual oscillations.

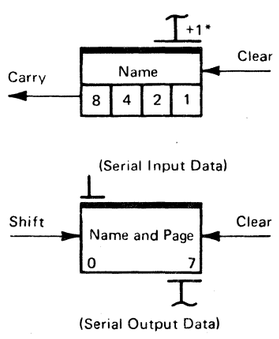
C: Indicates the presence of short pulses.

Logic Diagrams



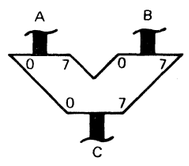
DECODE
Example shows decode of positions 5, 6, 7.

REGISTER
Symbol (■) means that register is displayed.



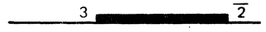
COUNTER
* Counter advance pulse is + for UP count — for down.

SHIFT REGISTER
Serial data enters at high-order bit position and is shifted toward low order bit position. Serial data exits at low-order bit position.



ADDER
A + B = C

Timing Charts



ACTIVE STATE
Numerals at the beginning and end of the bar identify the signals (numbered on the same chart) that activate and deactivate this line. A bar over the numeral (2) indicates that the lack of the signal activates or deactivates the line. The active-state bar indicates the polarity shift.

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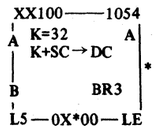
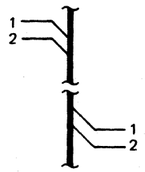
LEGEND (Part 2 of 6)

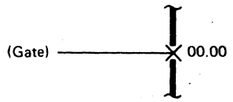


MICROPROGRAM INSTRUCTION EXAMPLE

Add 32 to contents of SC register and place results on D bus only. "C" causes ST3C to be turned on if there is a carry out of ALU.

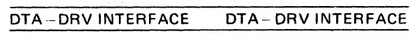


MULTIPLE LINE TRANSFER

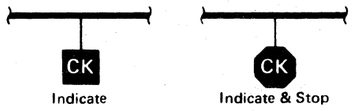


GATE

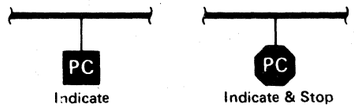
Numerals against gate symbol give page or diagram number of gating circuit.



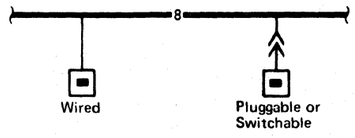
INTERFACE BETWEEN TWO FUNCTIONAL UNITS



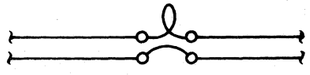
CHECK



PARITY CHECK



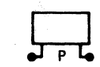
INDICATABLE BUS WITH NUMBER OF BUS LINES SHOWN



INTERBOARD CONNECTOR

SOLENOID

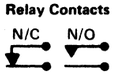
Identified by name, e.g., Feed Clutch.



RELAY OR CONTACTOR

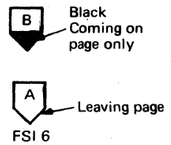
Type indicated by letter code.

P = Pick H = Hold
PL = Pick Lower LP = Latch Pick
PU = Pick Upper LU = Latch Upper



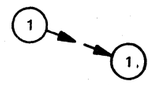
RELAY CONTACTS

Shown in the deenergized position.
N/C = Normally Closed (break).
N/O = Normally Open (make).



EXTERNAL PAGE CONNECTOR

Indicates connection between diagrams on separate pages. Letter keys are used to identify corresponding points. Below the symbol is the page number of the connecting point.



INTERNAL PAGE CONNECTOR

Indicates connection between several parts of the same diagram. Line-of-sight arrows assist in locating other connector(s).

TEST POINTS

All three are used throughout the manual. The waveform in the symbol is never intended to represent any real waveform to be displayed.

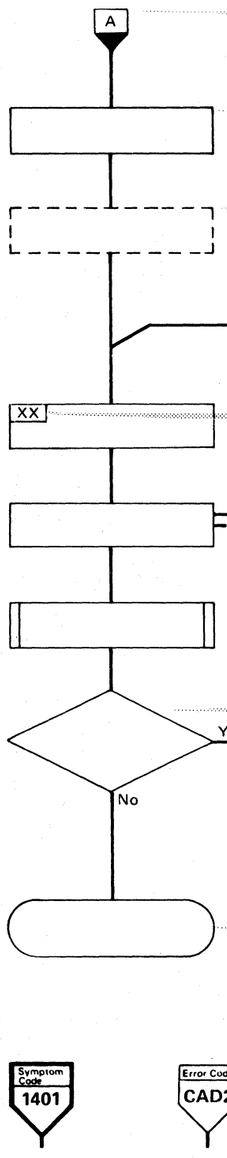
These symbols are used to highlight component installations, removals, adjustments, and measurements.

INSTALLATIONS AND REMOVALS

ADJUSTMENTS

MEASUREMENTS-CHECKS

Flowcharts



PROCESS, MAJOR FUNCTIONS OR EVENTS

EXTERNAL PAGE CONNECTOR (Entry)

Indicates entrance from correspondingly lettered symbol on referenced page.

BASIC ACTION BLOCK

ANNOTATION (In-Line)

Gives descriptive comment or explanatory note.

INTERNAL PAGE CONNECTOR

Internal page connector shows entry from correspondingly-numbered symbol elsewhere on page. Flow is top to bottom from the reentry point.

XX identifies register used for function or event.

ANNOTATION (Supplementary)

Gives descriptive comment or explanatory note.

FUNCTION OR PROCESS DETAILED ELSEWHERE

Block identifies process and indicates where the detailed flowchart is located.

DECISION

Indicates a branch to alternate paths.

EXTERNAL PAGE CONNECTOR (Exit)

Indicates exit to correspondingly lettered symbol on referenced page.

TERMINAL

Indicates beginning or end of flow path.

SPECIAL EXTERNAL PAGE CONNECTORS (Entry)

Symptom Code: Developed from sense information.

Error Code: Used with microdiagnostics.

Note: See MICFL section for special flowchart symbols used in that section.

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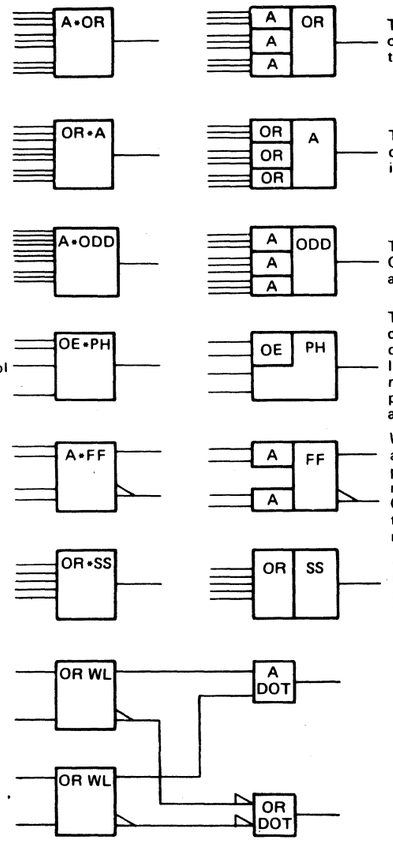
LEGEND (Part 3 of 6)

SOLID LOGIC DESIGN AUTOMATION

2 Level Symmetrical

Macro Symbol | **Butted Block (FEDA)**



The output line will be at its indicated polarity when one or more of the input AND groupings has all its inputs at the indicated polarity.

The output line will be at its indicated polarity when all of the input OR groupings have one or more of their inputs at the indicated polarity.

The output line will be at its indicated polarity when an ODD number of its input AND groupings has all its inputs at the indicated polarity.

The output line follows the data input line when the control input line is at its indicated polarity and the data input grouping (OE) is satisfied. If the data input line remains constant, changes in the control line will not affect the output. If the control input line reverses polarity, the output will remain at the polarity it held at the moment the control line changed.

When the top AND input goes to the polarity shown, a pulse sets the circuit and produces output of the polarity shown. After set time, the top AND has no effect.
Output opposite the polarity indicated results when the bottom AND goes to the polarity shown. After reset time the bottom AND input has no effect.

When one or more of the input pulses change to its indicated polarity, the output line temporarily changes to the polarity shown for a period of time that is characteristic of the particular circuit.

When the output of a block enters both a DOT OR and a DOT AND, the letters WL (wired logic) are placed to the right of the primary block function symbol.
Basic blocks whose outputs are connected externally to perform an AND or OR-function are identified by an A or OR placed to the right of the primary block function symbol, replacing the WL.

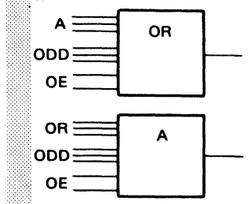
Note: Other functions may be dotted as shown in the chart below.

ADDITIONAL 2 LEVEL SYMMETRICAL

Input Level	Output Level	Symbol	Input Level	Output Level	Symbol
OE ODD OR	A	OE•A ODD•A OR•A	AND OE OR	PH	A•PH OE•PH OR•PH
AND OE	OR	A•OR OE•OR	AND OE OR	FF OR FL	A•FF A•FL OE•FF OE•FL OR•FF OR•FL
AND	ODD	A•ODD	AND OE OR	SS	A•SS OE•SS OR•SS
AND OR	OE	A•OE OR•OE			

Note: For additional information see IBM Maintenance Library, Logic Blocks, Automated Logic Diagrams SLT, SLD, ALST, MST, order number SY22-2798.

2 Level Asymmetrial



The output line will be at its indicated level when one or more of the input functions have been satisfied.

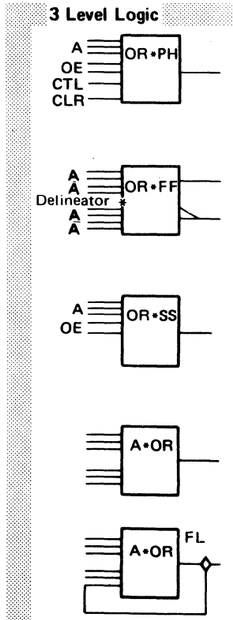
The output line will be at its indicated level when all of the input function groups have been satisfied.

ADDITIONAL 2 LEVEL ASYMMETRICAL LOGIC

Input Level	Output Level	Symbol	Input Level	Output Level		Symbol
*	AND	A	*	OE	*Any of the following functions: A, OR, AR, OE or ODD	OE
*	OR	OR	ODD	PH		PH
*	ODD	ODD	ODD	SS		SS

Note: For additional information see IBM Maintenance Library, Logic Blocks, Automated Logic Diagrams SLT, SLD, ASLT, MST, order number SY22-2798

3 Level Logic



The output line will be at its indicated polarity when one or more of the input functions are satisfied and the CTL input is at its indicated state. When the CTL input goes to the opposite polarity of that indicated, the output will hold whatever polarity it possessed. Activating the CLR input line resets the Polarity Hold circuit and the output will be reverse of the polarity shown.

The output lines will be at the indicated polarity when one or more of the input AND functions above the delineator has been satisfied. After set time the upper AND function has no effect.
Output opposite the indicated polarity results when the AND function below the delineator goes to the polarity shown. After reset time the lower AND function has no effect.

At the time one or both input functions is satisfied, the output line temporarily changes to the polarity shown for a period of time determined by the Single Shot (SS) block circuit.

DELINEATOR: The "*" will be inserted in the space reserved between top and bottom functional groupings.

The FL, PH and other symbols shall be placed as the top line output pin position where the macro symbol space requirement prohibits the dot function to be placed within the logic block.

Note: Other functions may be dotted as shown in the chart below.

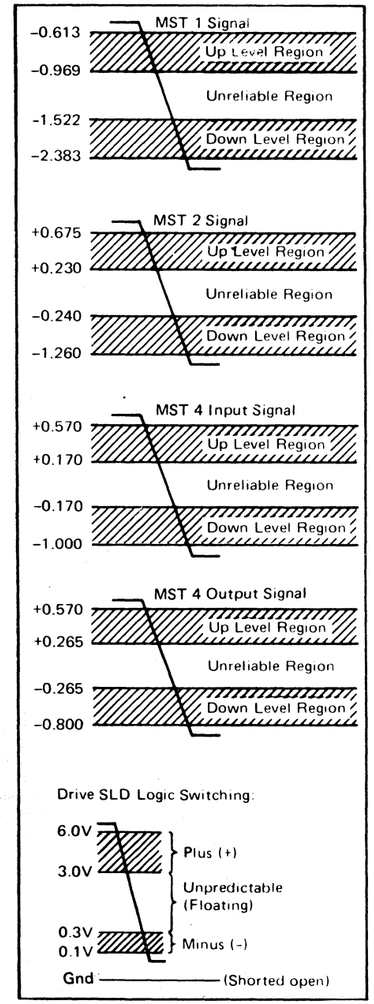
ADDITIONAL 3 LEVEL LOGIC

Input Level	Second Level	Output Level	Symbol	Input Level	Second Level	Output Level	Symbol
*	OR OE	A	OR•A OE•A	*	AND OR OE	FF or FL	A•FF A•FL OR•FF OR•FL OE•FF OE•FL
*	AND OE	OR	A•OR OE•OR	*	AND OR OE	SS	A•SS OR•SS OE•SS
*	OR AND OE	PH	OR•PH A•PH OE•PH	*Any of the following basic functions A, OR, AR, or OE.			

Voltage Levels

Technology	MST-1	MST-2	MST-4	
			Input	Output
MPUL	-0.613	+0.675	+0.570	+0.570
LPUL	-0.969	+0.230	+0.170	+0.265
LNDL	-1.522	-0.240	-0.170	-0.265
MNDL	-2.383	-1.260	-1.000	-0.800

MPUL = Most positive up level
LPUL = Least Positive up level
LNDL = Least negative down level
MNDL = Most negative down level



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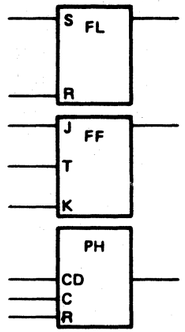
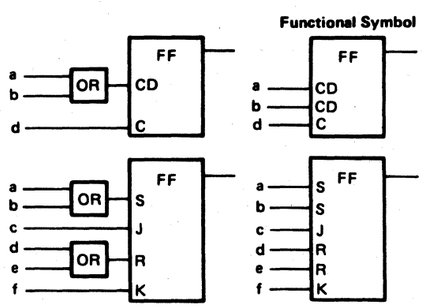
LEGEND (Part 4 of 6)

FUNCTIONAL SYMBOLS

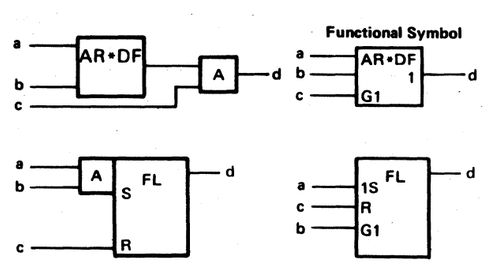
Descriptions



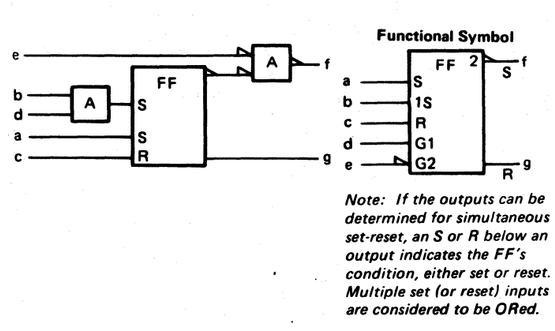
Basic Storage Symbols



Inherent-OR in the FF

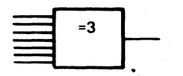


Single Function Application

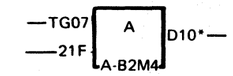


Note: If the outputs can be determined for simultaneous set-reset, an S or R below an output indicates the FF's condition, either set or reset. Multiple set (or reset) inputs are considered to be ORed.

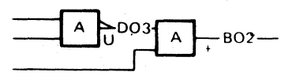
Dependent Notation



An equal sign (=) followed by a number specifies the number of input lines of the polarity shown required to produce the indicated output.



Note: An asterisk (*) on an input or output line denotes a connection that leaves the board, or refers to the connector listing at the bottom of the ALD page.



A plus (+) or minus (◺) under an output line indicates the extreme potential that may be forced by an external source.

A loading character (L or U) under the output line or in the edge of the block under the output line indicates that the external load cannot be isolated from the driving circuit without affecting the output of the driver.

Special Notations

STORAGE ELEMENT LINE DEFINITIONS

Inputs to storage blocks are identified by letters inside the block, adjacent to each input.

S	Set
R	Reset
J	Set (Complement)
K	Reset (Complement)
T	Complement
C	Control
CD	Controlled Data
G	Gating

The storage elements above show combinations of inputs.

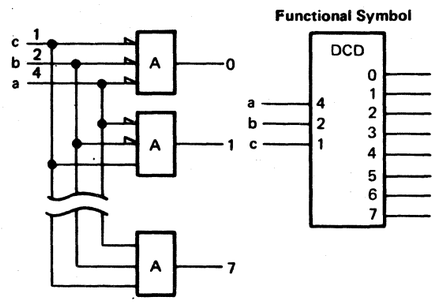
The storage elements (FL, FF, PH) show examples of the input line designations. The inputs are defined as follows:

S Set: When set is active, all outputs are at the polarity shown.
R Reset: When reset is active, all outputs are at a polarity opposite to that shown.
J Set: Acts as a set input, except that simultaneous application of J and K inputs will complement the output.
K Reset: Acts like a reset, except in combination with a J input.
T Complement: The T input complements each output.
C Control: When active, the control input permits the output to change with changes to the data input line. When inactive, the control line holds the output at whatever polarity it possessed at the moment the control line went inactive.
CD Controlled Data: When the associated control input is the polarity shown, a CD input at the polarity shown sets the storage element. Likewise, a CD input at its opposite polarity resets the storage element, when a control input is active. If multiple CD inputs to the storage element, any one active CD input can set the storage element.
G Gate: Represents the AND function without the use of the AND logic symbol. When multiple gating lines are required, gates are identified by the same numerals used to identify its related gated dependent line. A G1 gate will control an input or output line marked with a 1.

G Gate (input): When at the polarity shown will allow dependent inputs of the polarity indicated to affect the storage element. In all other cases it can be considered inactive.

G Gate (output): The dependent output will be at the polarity shown when the associated gating line is at its indicated polarity. In all other conditions the output stands opposite to the polarity shown.

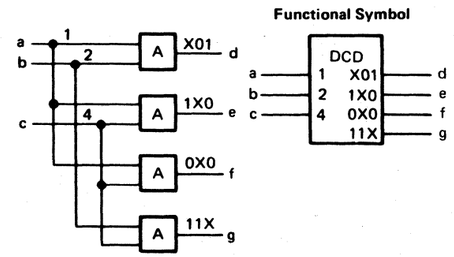
Decode



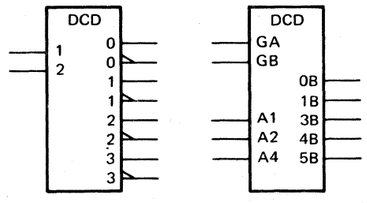
The decimal sum of the line values of those inputs which are at their active level equals the value of the active output line. If no input lines are active the 0 output line is active. If all input lines are active the 7 output line is active.

Note: The decimal sum value existing at the decoder inputs agrees with the decimal number shown at the output line labels. Only one output can be active at any given time.

Output Value	Input Line Condition
0	$\bar{a}$ $\bar{b}$ $\bar{c}$
1	$\bar{a}$ $\bar{b}$ c
2	$\bar{a}$ b $\bar{c}$
3	$\bar{a}$ b c
4	a $\bar{b}$ $\bar{c}$
5	a $\bar{b}$ c
6	a b $\bar{c}$
7	a b c



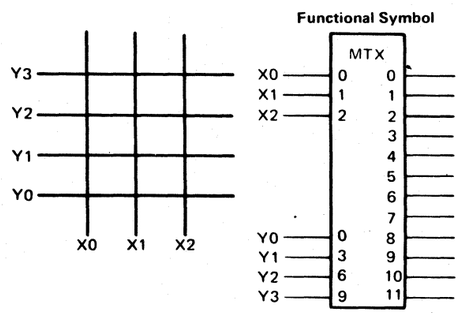
Note: Rightmost digit on the output line corresponds to the topmost digit on the input line ("X" in any position means that input line has no effect).



Multiple output lines can be associated with a given output (sum).

A decoder shown with gating lines.

Matrix



Active Input Lines							Active Output
X0	X1	X2	Y0	Y1	Y2	Y3	
X			X				0
	X		X				1
		X	X				2
X				X			3
	X			X			4
		X		X			5
X					X		6
	X				X		7
		X			X		8
X						X	9
	X					X	10
		X				X	11

Note: The matrix (MTX) is a functional logic block with two or more groups of inputs. The decimal numbered output will be active when it equals the decimal sum of one active line from each input group (shown in Chart). If any input group does not have an active input, then there is no active output from the matrix block.

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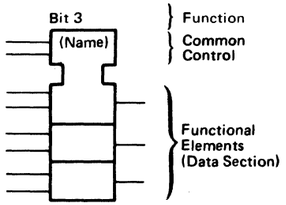
ELEMENTS WITH COMMON INPUTS/OUTPUTS (Part 1 of 2)

Element Description



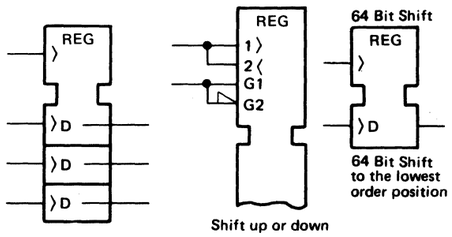
COMMON CONTROL SECTION: Used only for dependency (gating) and/or common lines for the register. There are no outputs from the common section.

NAME: May be any of the following: selector (SEL), register (REG), decoder (DCD), matrix (MTX), multiregister (MREG), and delay (DLY).

DATA SECTION: A group of vertically stacked functional elements. The number of stacked elements will vary with the number of inputs.

Note: The function of the logic element may be placed above the common control section outside the logic block.

Shift Register (REG)



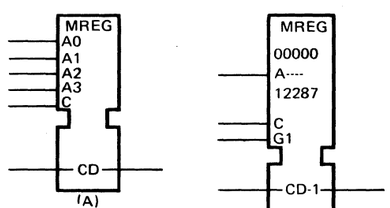
DEFINITION: The control input causes the data in each bit position to shift one position as indicated by one of the following designations.

" ⟩ " (greater than) When this line goes active the data content will shift from the top (uppermost) bit position. Similarly, the contents of each bit position will shift down the symbol.

" ⟨ " (less than) When this line goes active, the data content will shift from the bottom to the next bit position above and similarly for each bit position in the shift register symbol.

Note: A time difference in shifting will be indicated by a trailing edge symbol (¬).

Multi-Register (MREG)



Address notation A, AR, or AW must prefix the data. This indicates the data is dependent on an address.

A = Read Only Storage (ROS) or when the read/write address is identical.
AW = Write address. AW must be shown as data input dependent; (for example, AWCD).
AR = Read address. AR must be shown as a dependency with the output.

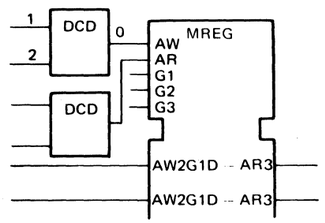
The numeric address span shall be specified in the common section.

"G" will replace the C to control the data information in the MREG. The C is reserved for the condition that would place a zero in all storage cells not addressed.

Example	Input Lines Needed	Output Lines Needed
(A)	A(0, 1, 2, 3) C CD	A(0, 1, 2, 3) CD (data)
(B)	A(0-12287) C CD	A(0-12287) G1 (gate) CD (data)
(C)	AW(0, 1, 2, 3) CD	AR(0, 1, 2, 3) CD (data)
(D)	AW(0-255) CD	AR(0-255) CD (data)

ORDER AND SELECTION OF FUNCTIONAL SYMBOLS HAVE THE FOLLOWING EFFECT

Note: No writing will take place in the addressed storage cell unless G1 is active. No readout will occur from the decoded address unless G3 is active.



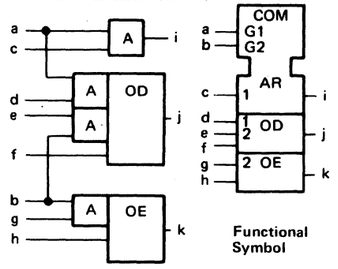
G1 Active at its indicated polarity:

(a) Data and G2 active with a decoded address = write a one

(b) Data or G2 inactive for a decoded address = write a zero

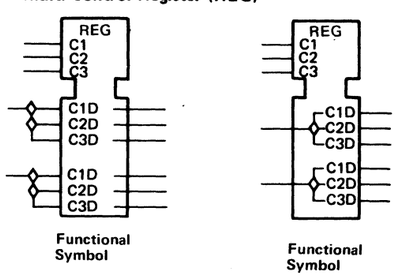
Note: The output will be active from a decoded address if a one had been stored in the storage element and G3 is active. If a zero had been stored or G3 is inactive, the outputs will be inactive.

Common Function (COM)



DEFINITION: Common Function block may be associated with any group of basic logic elements functionally related by their dependent gating. Each functional element shall contain the proper letter(s) that makes it an approved logic symbol. The common section may contain the letters COM at the very top line.

Multi-Control Register (REG)



The multiple control inputs shall be designated by sequential numbers shown entering the common section; for example, C1, C2.

The control data shall enter the data section of the symbol and will normally be diagrammed as multiple outputs.

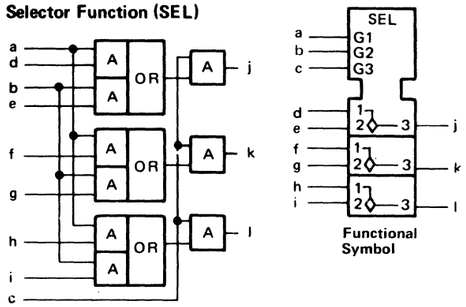
The "C" designator must be a suffix to differentiate it from a gate.

Example:

CID = Storage Data output controlled by C1.

Note: The "◇" symbol represents the OR function connection in the data section.

Selector Function (SEL)



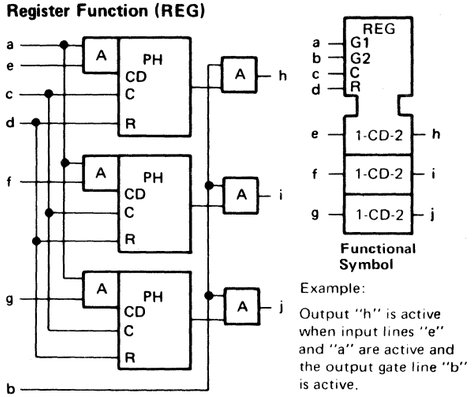
DEFINITION: A selector is a functional logic block consisting of two or more OR blocks having input and/or output signals dependent upon common gates.

Example:

Output line "j" is active when line "c" is active and lines "d" and "a" or lines "e" and "b" are active.

Note: The "◇" symbol represents the OR function connection in the data section.

Register Function (REG)



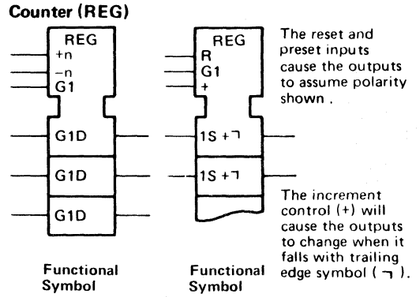
Example:

Output "h" is active when input lines "e" and "a" are active and the output gate line "b" is active.

DEFINITION: A register logic block consisting of a group of associated storage elements with common input and/or output gating or other common input lines such as reset.

Note: Descriptive nomenclature such as bit 1, may be placed above each logic element.

Counter (REG)



DEFINITION: A Register to be incremented or decremented under control of input lines drawn to the common section of the symbol with the follow notations.

"+n" When this line goes to its indicated polarity the decimal quantity n is added to the binary count contained in the register. The n need not appear when it is a one.

"−n" When this line goes to its indicated polarity, the decimal quantity n is subtracted from the binary count contained in the register, The n need not appear when it is a one.

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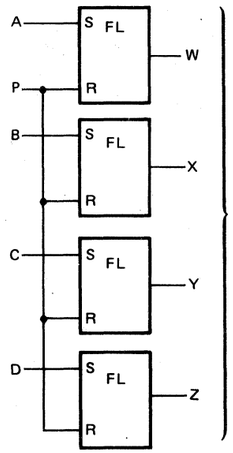
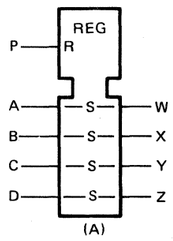
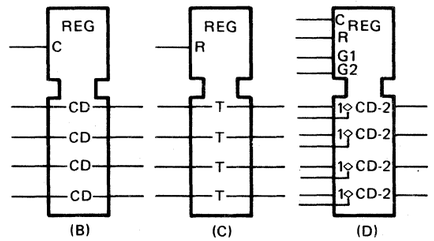
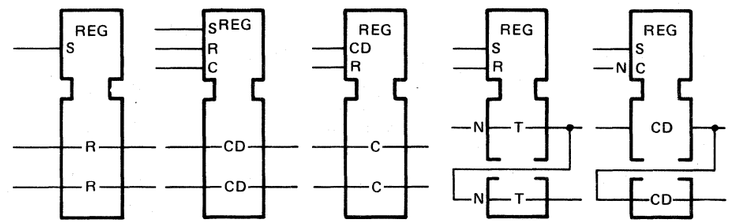
ELEMENTS WITH COMMON INPUTS/OUTPUTS (Part 2 of 2)









Note: See LGND 12 for storage element line definitions: S, CD, T, R, C, G etc.

Example A shows four FL blocks with a common reset.

Example B shows four PH blocks with a common control line.

Example C shows four FF blocks with a common reset.

Example D shows a register with gate. The G1 gate-in line is needed to set bits into the register (upper set of inputs); ORed with each of these inputs (by a diamond) is an ungated input. The G2 gate-out line is necessary to produce an output.

Example E shows a set line common to two positions.

Example F shows two data positions capable of being set or reset by a single S or R input.

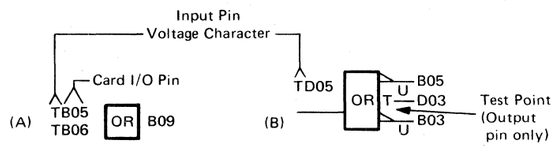
Example G shows a data line common to more than one control input; whatever data is available at CD is stored into a position when the appropriate C input is active.

Example H shows a multiposition register in which the state of a position depends on the data stored in the previous position. In the example, each position can be set or reset by the common S or R line. Whenever a negative shift appears at the input to the first position, the position complements; the second position, likewise, complements only if the first position changes from plus to minus.

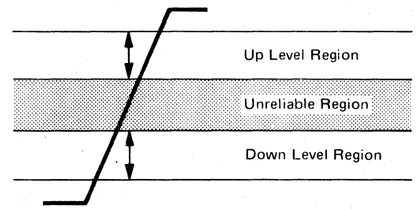
Example J is similar to H except that CD lines appear in the data section. At any time, the data available to the first position is stored in that position (and reflected at its output) when the control line shifts negatively. All remaining positions of the register store the data available at the immediately previous position. *Note:* The N external to the block indicates that a negative pulse or shift activates the control line (nonstandard).

Note: The "◇" symbol represents the OR function connection in the data section of the logic block.

Voltage Codes

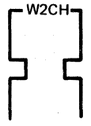


Input Pin Voltage Code	Minimum Up Level Region	Minimum Down Level Region
B	2.5 to 2.1	1.9 to 1.5
C	2.5 to 2.1	1.4 to 1.0
D	1.9 to 1.6	1.4 to 1.0
E	2.0 to 1.6	0.9 to 0.6
F	4.0 to 3.5	0.5 to 0.3
G	2.5 to 2.1	0.5 to 0.3
H	2.0 to 1.6	0.5 to 0.3
J	1.5 to 1.1	0.5 to 0.3
L	0.7 to 0.5	0.4 to 0.2
T	0.3	−0.3
Z	−1.0	−1.5



Additive Card Code

Line 1 (top line) of the logic block contains the additive card code. The additive card code may contain as many as four characters. The additive card code identifies the logic associated with special features and unique functions. See example.



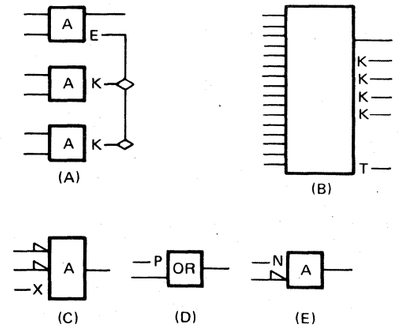
W2CH = With 2 channel switch.
W4CH = With 4 channel switch.
OPF- = Optional feature (not designated).
WM4K = With more than 4K of memory.
WISC = With integrated storage control.
NISC = Not integrated storage control.
N2CH Not 2 channel switch.

Edge of Block Character

An edge of block character, alongside or in the edge of an FEALD (MST) block, serves the following functions:

Example A	E	An extender. In combination with a K output, shows that additional blocks act as inputs to the first block.
Example A	K	At the output of a block, a K can connect to another K output or to an E output; these K "outputs" are actually inputs to the first block (with the output E) and extend its function.
Example B	K	At times, the number of inputs to a logic block exceeds design automation program capabilities. In this case, the excess inputs are shown as outputs but identified with the letter K.
Example C	X	A nonlogic input or output. The driving circuit to this input is usually a fixed voltage or bias. An X line does not influence the state of a circuit.
Example D	P	A positive-going shift or pulse activates the block.
Example E	N	A negative-going shift or pulse activates the block.
Example B	T	A test point. Do not confuse this with T as an input voltage character.

Note: U (unloaded) may be used in the edge of a block below the line affected. See LGND 12 for definition.



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ABBREVIATIONS AND DEFINITIONS (Part 1 of 3)

A

A	AND function; Amperes
A*OR	AND-OR function
ACR	Address Compare Register
ADDRO	Address Out (Branch Indicator)
ADD, ADR, ADDR	Address
AGC	Automatic Gain Control
ALD	Automated Logic Diagram
ALT	Alternate
ALU	Arithmetic Logic Unit
AM	Address Marker
APC	Angular Position Counter
AR	Amplifier (Logic block)
AR-MD	Amplifier, Magnet Driver (Logic block)
ARGUMENT	A bit configuration that bears specific control information
ASLT	Advanced Solid Logic Technology
ASM, ASY, ASSM	Assembly

B

B	Blower, air
BAR	Backup Address Register
BBCCHH	Bin (2 bytes), Cylinder (2 bytes), Head (2 bytes)
BCD	Binary Coded Decimal
BDY-2	Boundary 2 (Branch Indicator)
BFRDY	Buffer Ready
BIN	Binary
BLK	Block
BOPAR	Bus Out Parity (Branch Indicator)
BOUNDARY	Limit or extent as: a Word Boundary
BR, BRCH	Branch
BSCA	Bit Significant Controller Address
BSDA	Bit Significant Device Address
BSM	Basic Storage Module
BTRDY	Byte Ready
BTU	British Thermal Units
BUF, BFR	Buffer
BUFUL	Buffer full
BYTE	Eight bits plus a parity bit

C

C	Capacitor: coulombs
CA	Microinstruction field that is decoded to select a GP register to serve as A-entry register
CAR	Cylinder Address Register
CAS	Control Automation System; Compare Address Switches
CB	Circuit Breaker; Microinstruction field that is decoded to select a GP register to serve as B-entry register
CC=3	Condition Code 3
CCB	Correction Code Byte
CCC	Correction Code Check
CCHH	Cylinder (2 bytes), Head (2 bytes)
CCHHR	Cylinder (2 bytes), Head (2 bytes), Record (1 byte)
CCU	Common Control Unit (Same as CU, SCU)
CCW	Channel Command Word
CD	Microinstruction field that is decoded to select a GP register to serve as destination register; Core driver
CDS	Configuration Data Set
CE	Customer Engineer; Channel End
CEB	Command Execution Byte
CFEALD	Condensed Field Engineering Automated Logic Diagram
CH	Microinstruction field that is decoded to select a hardware branch condition
CH, CHL, CHAN	Channel
CHAINING	Sequential linking of instructions or data
CHANB, CHB	Channel B
CHK-1	Check 1
CHK-2	Check 2
CHKA	Check A
CHL-I	Channel Interface
CI, CTL-I	Control Interface
CIB	Compressed Index Block
CK	Microinstruction field the contents of which are gated to the A-register
CKD	Count-Key-Data
CL	Microinstruction field that is decoded to select a hardware branch condition
CLD	CAS Logic Diagram
CLK	Clock
CM	Centimeters; Control Module
CMMD, CMD	Command
COM	Common Function (Logic Block)
COMMO	Command Out (Branch Indicator)
COMP	Compare
COND	Condition
CP	Circuit Protector
CPU	Central Processing Unit
CR	Diode; rectifier (semiconductor)
CRY	Carry
CS	Current Switch; Microinstruction field that is decoded to set or reset specific ST register bits
CSW	Channel Status Word
CTL-I, CI	Control Interface
CTR, CNT	Counter, Count
CTRL	Control
CU	Control Unit (Same as CCU, SCU)
CUDI	Control Unit Device Interface
CUEND	Control Unit End (Branch Indicator)
CURR	Current
CW	Microinstruction field, the contents of which are gated to IAR high; Converter (Logic block)
CX	Microinstruction field, the contents of which are gated to IAR high and the A register. Microinstruction field, the contents of which are gated to IAR low
CYC	Cycle
CYLINDER	A vertical surface formed of tracks on a storage device that can be accessed without repositioning the access mechanism

D

DAR	Data Address Register
DASD	Direct Access Storage Device
DCC	Disconnected Command Chain
DCD	Decoder (Logic Block)
DCI	(See CI – CTL-I)
DDA	Direct Disk Attachment (125)
DE	Device End
DEC	Decode
DEC0	Decode Time 0 (Branch Indicator)
DELTA, Δ	A three-terminal circuit configuration (usually refers to the primary winding arrangement of a transformer). Also used to indicate a change in some dimension, such as: Δt = change in time; Δd = change in distance
DEV	Device
DF	Differential Amplifier
DIAG	Diagnostic
DIFF	Difference Counter
DISC	Disconnect
DISP	Display
DL	Data (area) length
DLY	Delay (Logic Block)
DLYD	Delayed
DM	Data Module
DO	Data Out
DRV	Drive
DS	Lamp (indicator)
DVM	Digital Voltmeter

E

EC	Edge connector; Engineering Change
ECC	Error Correction Code
ECD	Error Condition (check) Diagram
EDI	Expected Device Interrupt
EL	Error Log
ENTR	Entry
EOF	End of File
EREP	Environmental Record Edit and Print
ERP	Error Recovery Program
ERR	Error
EV	Even (Logic Block)
EXPTD	Expected
EXT	External

F

F	Flag; Fuse; farads (capacitor)
FCCHH	Flag (1 byte), Cylinder (2 bytes), Head (2 bytes)
FEALD	Field Engineering Automated Logic Diagram
FET	Fetch
FF	Flip-Flop (Logic block)
FL	Flip Latch (Logic block); Filter
FM	Microinstruction bit that is decoded to perform a specific CU gating function that determines format; Frequency Modulator; File Mask
FRU	Field Replaceable Unit
FSC	Fault Symptom Code
FSI	Fault Symptom Index

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ABBREVIATIONS AND DEFINITIONS (Part 2 of 3)

G

G	Giga – (10^9); grams
G1	Gap between index point and R0
G2	Gap between count area and key area
G3	Gap between data area and address marker of the following record
G4	Gap after data area of the last record on a track
GEN	Generator
GND	Ground
GPR	General purpose register

H

H	Henries (measure)
HA	Home address
HAR	Head Address Register
HARD ERROR	A malfunction that is detected internally and considered to be of a catastrophic magnitude
HARDCORE TEST	Diagnostic to test the basic function of circuits and design
HD	Magnetic head driver
HDWARE	Hardware
HEAD	An electromechanical device that records, reads, or erases a storage medium
HEX	Hexadecimal
HIO	Halt Input/Output command
HLTIO	Halt Input/Output (branch indicator)
HP	Horsepower
HR	Heater
HS	Heat sink; high speed
Hz	Hertz

I

IAL	Low-order byte of the Instruction Address register
IAR	Instruction address register
ID	Identifier; indicator driver
ILXEQ	Inline execute
IMPL	Initial microprogram load
INCR	Increment; increase
IND	Indicate; indicator
INIT	Initiator
INLIN	Inline
INSTR	Instruction
INT	Internal
INTF, IFC	Interface
INTR	Introduction
IO,I/O	Input/output
IPL	Initial program load
ISCB	Initial selection control block

J

J	Connection, receptacle; jack plug
JCL	Job control language
JMPR	Jumper

K

K	Key; Relay (contactor), kilo(10^3), 1024(2^{10})
KD	Key-data
KK	Microinstruction bit that is decoded to perform a specific CU gating function that determines format
KL	Key (area) length

L

L	Latch; inductor
LTCH, LTCHD	Latch, latched
LAP	Logical address plug
LB	Laminar bus
LD	Load; line driver
LDI	Logical device indicator
LIM	Limiter (logic block)
LR	Line receiver (logic block)
LT	Line terminator (logic block)

M

M	Meter; meters (measure); mega –(10^6); milli – (10^{-3})
MACH	Machine
MAL	Monolithic array logic
MAP	Malfunction analysis procedure
MAX	Maximum
MCI	Miscellaneous control information
MC6	MC Reg Bit 6 (branch indicator)
MC7	MC Reg Bit 7 (branch indicator)
MD	Magnet Driver
ME	Microinstruction bit that is decoded to perform a specific CU gating function that determines format
MFM	Modified frequency modulator
MFT	Multiprogramming with a fixed number of variables
MH	Microinstruction field whose contents are gated to DAR high
MIC, MICRO	Microprogram, microdiagnostic
MIN	Minimum; minutes
ML	Microinstruction field whose contents are gated to DAR high
MLM	Maintenance Library Manual
MLX	Maintenance library cross reference index
MODULE	A functional unit built to operate with other components
MPL	Microprogram load
MREG	Multiregister (logic block)
MSG	Message
MST	Monolithic System Technology; master
MT, M/T	Multiple track
MTX	Matrix (logic block)
MULTAG	Multiple tags
MULTI	Multitag switch on (branch indicator)
MVT	Multiprogramming with a variable number of tasks
MXT	Multiple exposure table

N

N	Inverter (logic block); nano – (10^{-9})
N OR	Inverter-OR (logic block)
N/O	Normally open point
N/C	Normally closed point
NB	Microinstruction bit that is decoded to perform a specific CU gating function that determines format
ND	Microinstruction bit that is decoded to perform a specific CU gating function that determines format
NEG	Negative
NH	Microinstruction field whose contents are gated to DAR low
NL	Microinstruction field whose contents are gated to DAR low
NO-OP	No Operation
NORM	Normal

O

OBR	Outboard recording
OD	Odd (number)
ODE	Outstanding device end
OE	Exclusive-OR function
OEC	Orientation execution code
OFFLINE	Isolated control of a unit from a primary function
OLT	Online test
OLTEP	Online test executive program
OLTSEP	Online test standalone executive program
ONLINE	The unit is available to a primary function
OP	Microinstruction field that is decoded to specify an ALU function; Operation; operating point
OPT	Option
OR	OR function
OR*FL	OR-flip-latch function
OS	Operating system
OSC	Oscillator
OVERRUN, OVRN	Overrun may occur if Service Out of Data Out is not received by the Control Unit within a specified time after Service In or Data In is presented to the channel.

P

P	Plug (connector); pico –(10^{-12})
PAR	Parity
PARAMETER	A constant value for a given purpose
PC	Parity check
PCH	Pack change
PCI	Program control interrupt
PERM	Permanent
PG	Parity generate
PGM	Program
PH	Polarity hold
PLD	Power line dip
PLO	Phase-locked oscillator
PLOT	Plug-on terminator
P/N	Part number
PROP	Propagate
PS	Power supply
PSIG	Pounds per square inch, gauge
PSW	Program status word
PU	Pick-up (magnetic head)
PWR, PWRD	Power, powdered

Q

Q	Transistor

3830-2

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Seq. 2 of 2	Part No. ( )	15 Aug 72	16 Oct 72	4 June 73	15 Apr 74			

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ABBREVIATIONS AND DEFINITIONS (Part 3 of 3)

R

R	Resistor; Record
R0	Record zero
R2	Resistor 2; record 2; relay 2
RAW DATA	Data as it is read from the storage medium
RCVR	Receiver
RD	Read
REG	Register
RESP	Respond
RESV	Reserved
ROS	Read Only Storage
RPS	Rotational Position Sensing
RSPON	Response (Branch Indicator)
RST	Reset
RTN	Routine
RW, R&W	Read/Write
RY	Relay, single coil
RY-CT	Relay, contact
RY-H	Relay, hold coil
RY-P	Relay, pick coil

S

S	Switch
SAL	Sense Amplifier Latch
S2	Sector 2
SCB	Sense Control Block
SCIB	Search Compressed Index Block
SCR	Silicon Controlled Rectifier
SCRID	SCR Indicator Driver
SCU	Storage Control Unit (Same as CU, CCU)
SD	Skip Displacement
SECTR	Sector
SEGMENT	Divided into significant units.
SEL, SELTD	Select, selected; Selector (logic block)
SEP	Separate
SEQ	Sequence
SER	Storage Error Register; serial
SERDES	Serializer/Deserializer
SERV	Service
SERVO, SERVOUT	Service Out
SFM	Set File Mask
SIM	Simulate
SIO, SI/O	Start Input/Output
SIP	Seek In Progress
SK	Seek
SLT	Solid Logic Technology
SO	Service Out
SOFT ERROR	Internally recoverable malfunction that is transparent to the user
SP, SPEC	Special; special function
SRL	System Reference Library
SS	Single-Shot (Logic block)
ST, STAT	Status, Status Register
STKD	Stacked
STOR	Storage
STP	Stop
SUPPO	Suppress Out (Branch Indicator)
SUPPR	Suppress
SW	Switch
SYNC BIT	Generated by the Control Unit during Read and Write operations
SYNDROME BITS	Corrects single bit errors and is used in detecting double bit errors

T

T000–T060	A specific clock time
T	Transformer
TACH	Tachometer
TAR	Temporary Address Register
TB	Terminal Board
TCS	Two-Channel Switch
TD	Time delay
TDR	Track Description Record (R0)
THRM	Thermal Element
TIC	Transfer-In-Channel
TP	Test Point
TRACK	A location on a storage medium accessable by one R/W head
TRAILING EDGE SYMBOL(¬|)	Activates a circuit on the fall of the designated signal
TRUNCATE	To end an operation before completing the function

U

U	Monolithic module
UDCD	Unit Data and Control Diagram
UC	Unit Check Status Bit
UCW	Unit Command Word

V

V	Voltage amplifier (Logic block)
VCM	Voice Coil Motor
VCO	Voltage Controlled Oscillator
VFO	Variable Frequency Oscillator

W

W	Bus Terminal; cable assembly; wire; watts
WCS	Writeable Control Storage
WL	Wire Logic
WORD	Four Bytes
WR, WRT	Write
WRAPAROUND	Advance according to some sequence with automatic restart provisions; jumpering of interfaces to run microdiagnostic tests
WYE, Y	A three-terminal circuit configuration (usually refers to the primary winding arrangement of a transformer)

X

X	Fuse holder; Lamp holder; socket
XEQ	Execute
XOR	Exclusive-OR function
XCHAN	Switched to channel C or D (Branch Indicator)
XFER	Transfer (Branch Indicator)

Y

Y	(See WYE)

Z

Z	Impedance network

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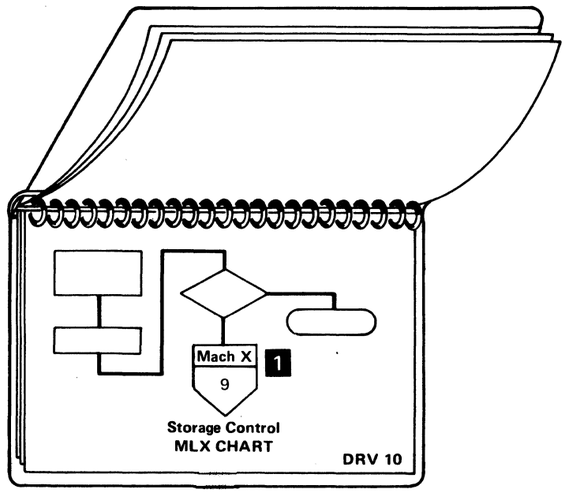
MAINTENANCE LIBRARY CROSS REFERENCE (MLX)

USE THIS PAGE WHEN ENTERING THIS MLM FROM ANOTHER MLM:

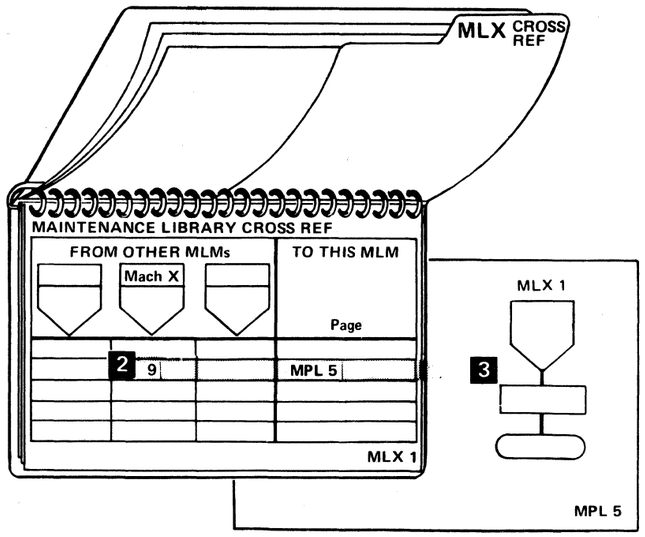
Note: Some MLMs do not use the MLX cross reference system.

1. Note exit number on page of MLM you are leaving.
2. Find that exit number in the appropriate column of the chart on this page.
3. Proceed to referenced page in this MLM.

Leaving Machine X Maintenance Library



Entering 3830-2 Maintenance Library



FROM OTHER MLMs						TO THIS MLM
			3350	3340	3333	Page
			1	1	1-37	START 10, Entry A
					40	START 90, Entry A
			11	11	44-46	START 10, Entry B
			5	5	47	START 90, Entry B
			9	9	56	SENSE 15, 20, 40, 45
			9	9	58	SENSE 10, 35, 40
			10	10		START 90, Entry C
						START 90, Entry D
			7	7		SENSE 25

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3830-2 MLM EXIT LISTING

USE THIS PAGE WHEN TRACING BACK FROM ANOTHER MLM TO LOCATE A LINE THAT EXITED FROM THIS MLM.

Exit	Page(s)
1	
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3	START 40
4	
5	START 15, 40, 45
6	MSG 20
7	MSG 20
8	MSG 20
9	START 10, 15
10	FSI 10
11	
12	START 10, FSI 5
13	
14	SENSE 10, 25, 30, 35, 45
15	FSI 15
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20	START 10, FSI 5
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START

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CE Initial Entry . . . . . START 10 ◀ *START MAINTENANCE HERE*
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MAINTENANCE PHILOSOPHY

- All problems are traced step-by-step through the procedures which begin on START 10.

- Solid and intermittent failures are detected by hardware and functional microprogram. Together they provide the means of retry and isolation of a failure to a functional area of the facility.

- Failures are categorized by their degree of impact on the storage facility operation:

CHECK 1 ERRORS

All errors detected in control storage and microinstruction control path are classified as Check 1 Errors. They are detected by hardware checking the circuitry and stop the control unit clock at the end of the cycle in which they are detected. Check 1 error data can be displayed on the CE panel. (See PANEL 40.) This type of error also appears as a Format 3 (selective reset) failure in sense data. (See SENSE 10.)

CHECK 2 ERRORS

All errors detected in the controller, control interface, drive, drive interface, channel interface, and file data path are detected by hardware and microprogram checking. (See PANEL 50.)

When the 3830-2 is running in CE Check Stop mode, the appropriate lamp on the CE panel (Check 1 or Check 2) indicates the type of failure.

- Check 1 and Check 2 errors, with the exception of correctable control storage checks, are logged in control storage and retrieved by the system's Error Recovery Program, if possible.

  The retrieved information provides sense data which identifies the failure. The sense bytes are in seven formats, four of which are available to the SCU (formats 0, 2, 3, 6). The other sense bytes are used for device sense data. Each format consists of 24 bytes with unique bit values. (See SENSE 10.)

  These unique bit values are decoded (FSI 5) into a fault symptom code (formats 0-4 only) which indexes the appropriate Analysis Procedure through the Fault Symptom Index (FSI).

- Every identifiable failure is covered in the analysis procedure as follows:

  1. Logic cards, when they are a possible source of the failure. The procedure suggests replacement of the failing card(s) during analysis if spare parts are available. If not, the failing card(s) should be swapped with one of like part number located elsewhere in the machine. Since indiscriminate card swapping can complicate the problem, card-level flowcharts and card contents are provided for your guidance (START 900-911).

  2. Instructions stating when and what microdiagnostics to run, including the operating procedure and error analysis.

  3. Error Condition Diagram (ECD), which depicts the logic that generated the error. The diagram will either be part of the analysis procedure or referenced when it appears elsewhere in the Maintenance Library. Should card replacement not correct the error, the ECD provides the next level of information to continue the analysis.

- Several methods are available for obtaining error analysis information. Listed below is the preferred method of error analysis and the resulting impact on the system.

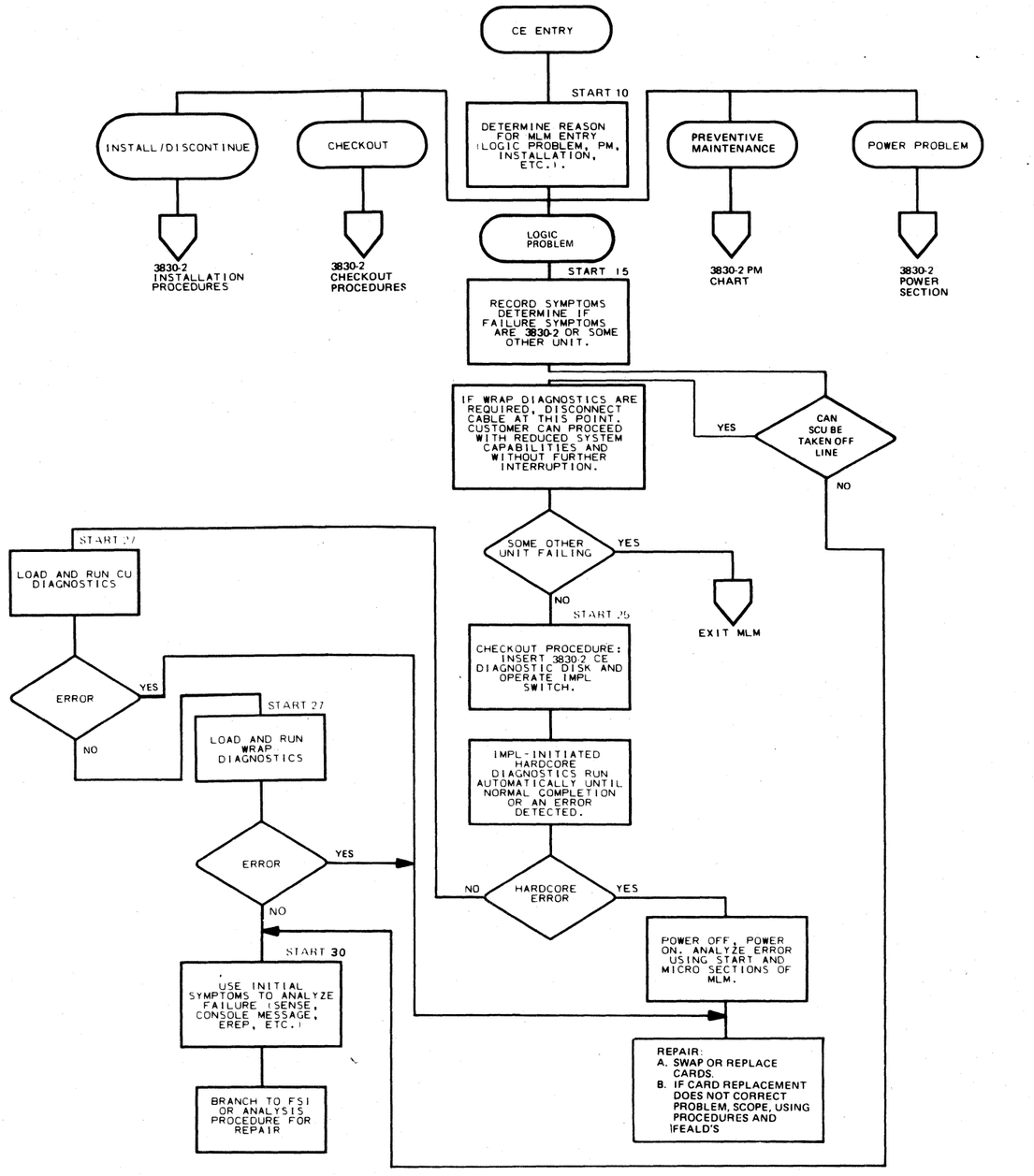
  1. Run microdiagnostics from the SCU CE panel. Facility is offline. Remaining system is available to customer. See START 25, entry A and START 27, entry B.

  2. Obtain EREP or console message printouts from the operating program (see MSG Section). There will be slight system impact during printing.

  3. Rerun the customer's job that failed. If operating system is capable of multitasking, customer operations may be run concurrently.

OVERALL DIAGNOSTIC PROCEDURE

For information only!
Use START 10 for maintenance.



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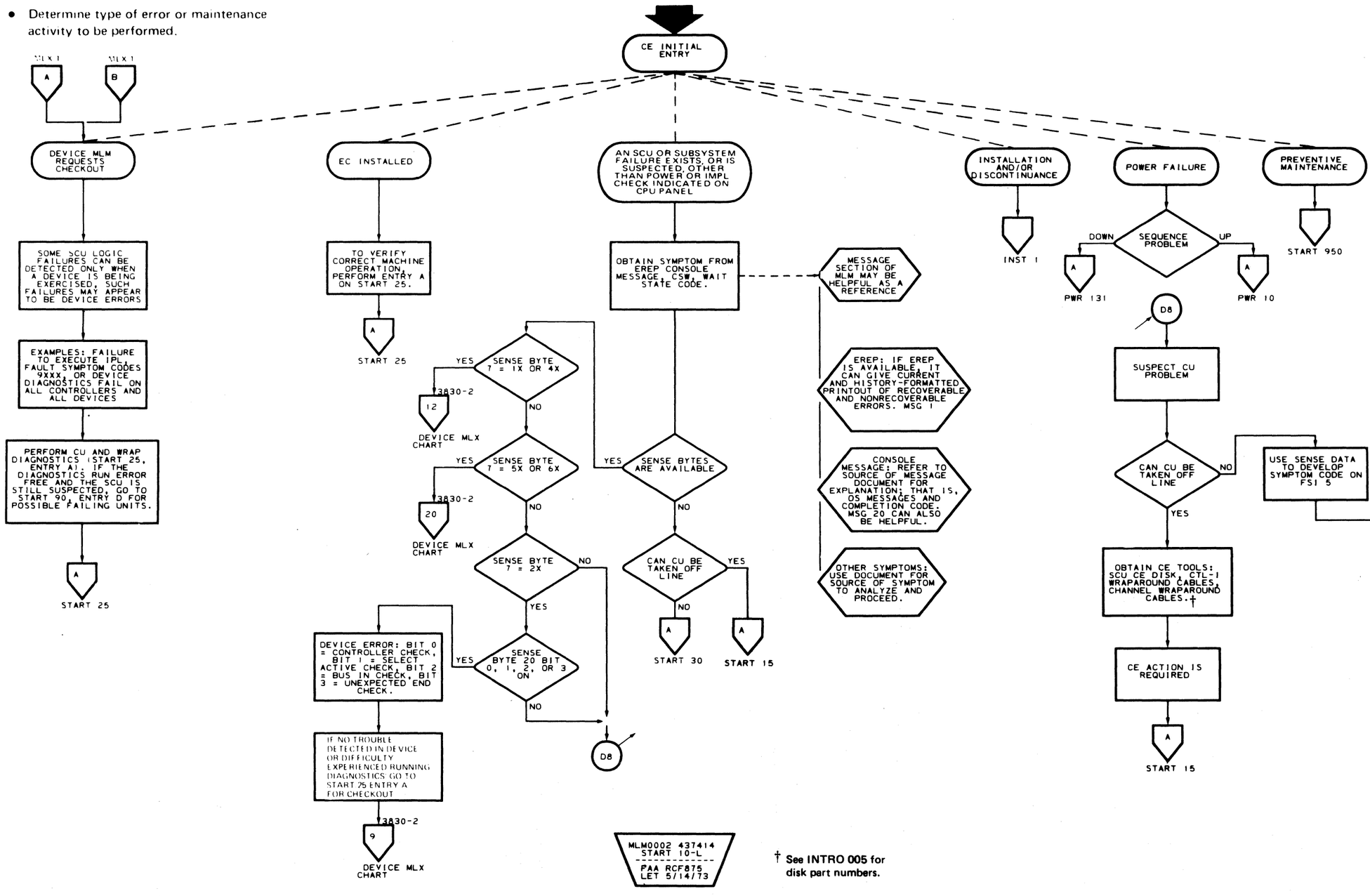
CE INITIAL ENTRY

- Entry point to maintenance package
- Determine type of error or maintenance activity to be performed.



† See INTRO 005 for disk part numbers.

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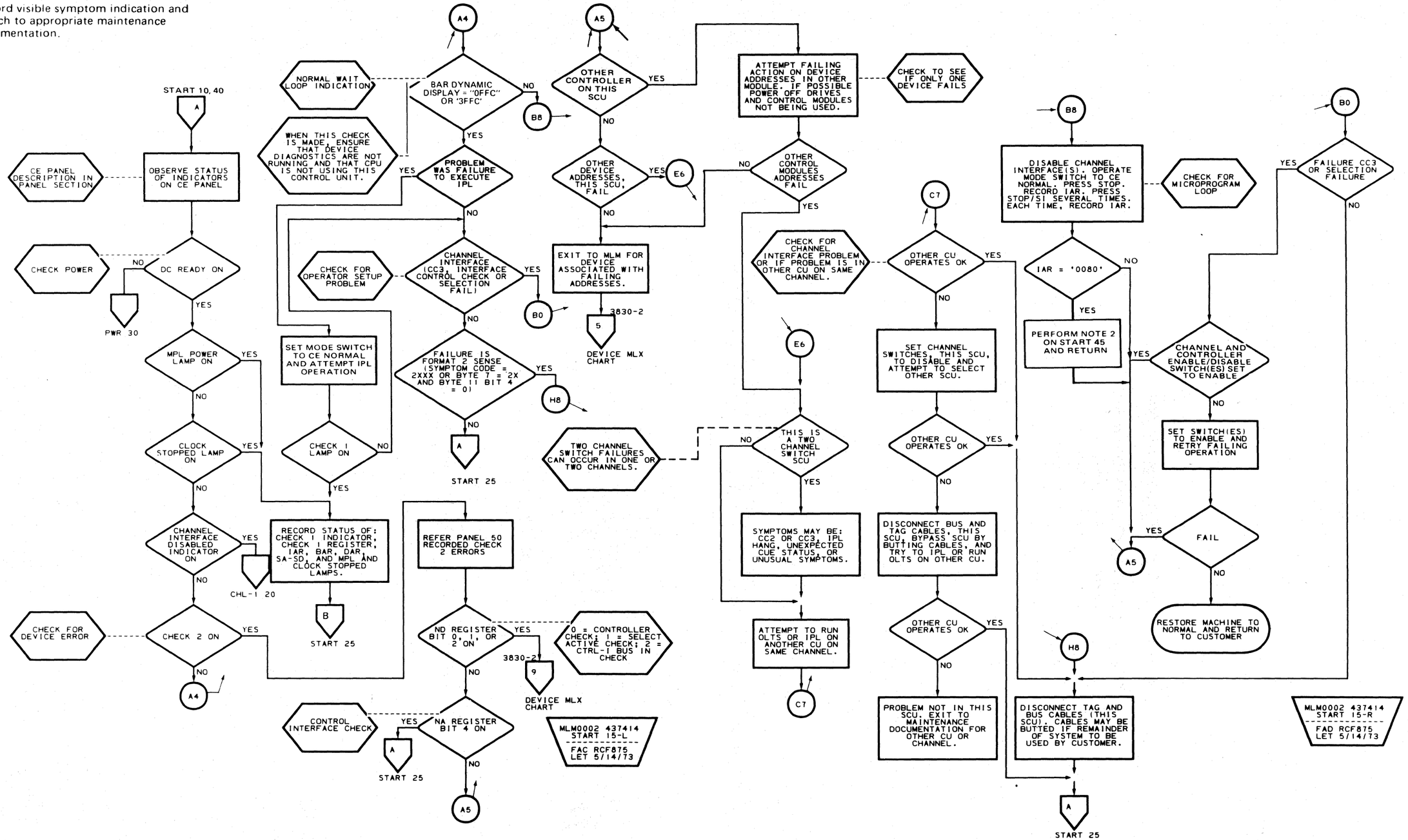
ERROR IDENTIFICATION

- Record visible symptom indication and branch to appropriate maintenance documentation.



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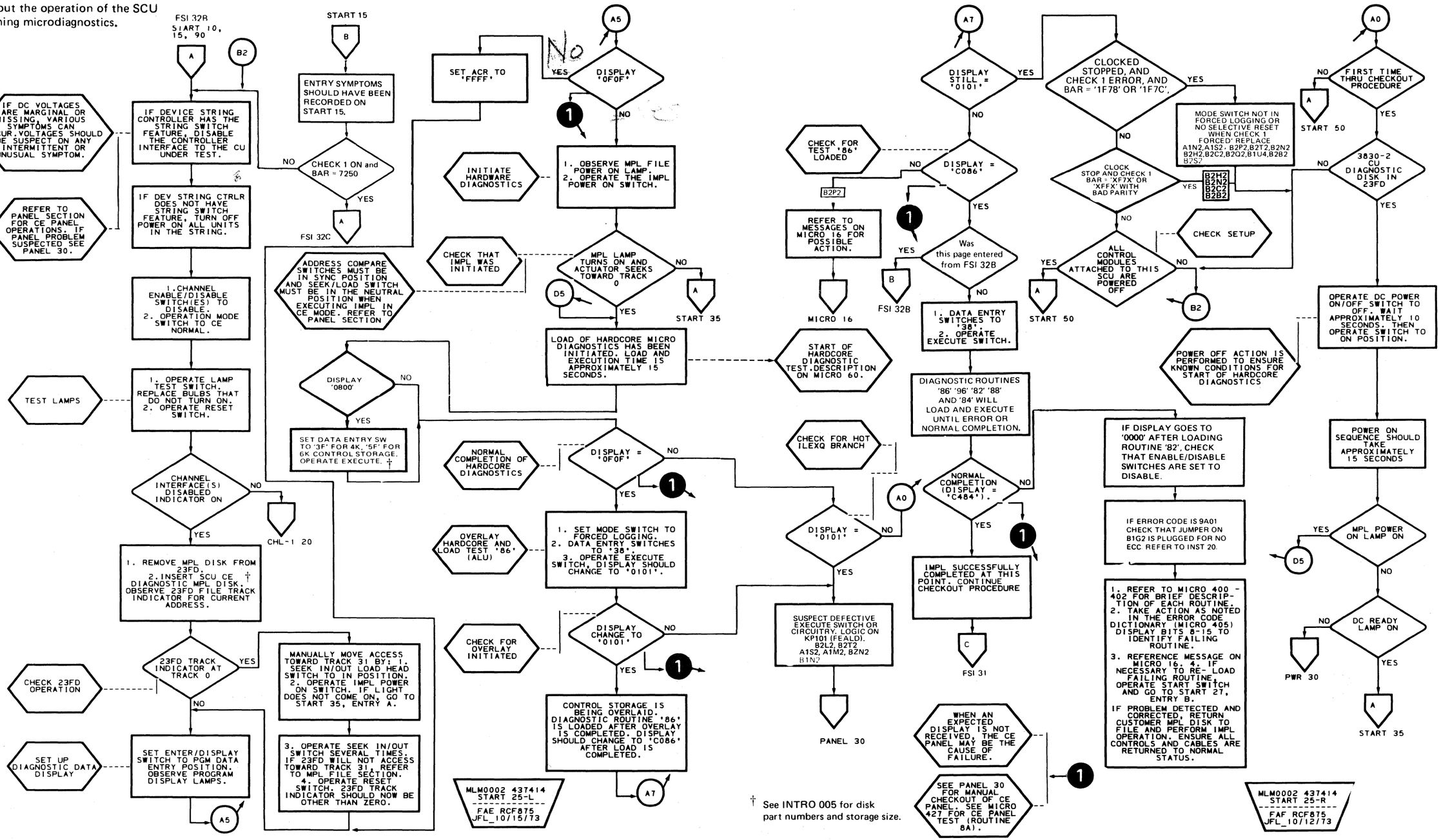
CHECKOUT PROCEDURE (COP) (Part 1 of 2)

- Check out the operation of the SCU by running microdiagnostics.



† See INTRO 005 for disk part numbers and storage size.

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CHECKOUT PROCEDURE (Part 2 of 2)

B START 55

Note: 3830-2 CE diagnostic disk must have been inserted and IMPL successfully executed using procedures on START 25 before the following procedures are attempted.

1. Operate the Mode switch to **Forced Logging** position.

   Note: Refer to PANEL section for CE panel operations. If panel problems are suspected, see PANEL 30.

2. Load and run microdiagnostics in the following sequence (loading instructions are on MICRO 15 and 16):

Routine	Description	Operating Instructions
86	ALU Functions (links to Routine 96)	MICRO 20
96	F Reg Control (links to Routine 82)	MICRO 20
82	Register Test (links to Routine 88)	MICRO 20
88	Control Storage Pattern Test (links to Routine 84)	MICRO 20

Refer to MICRO 400 for brief description of each routine. If an error occurs, take action as noted in the Error Code Dictionary (start at MICRO 405). If routines cannot be loaded and hardcore runs error free, go to PANEL 30 (CE Panel Checkout).

84	Check of Checkers and Control	MICRO 410
8A	CE Panel Test (This test should be run for CE Panel checkout or CE Panel suspected problems only.)	MICRO 427

3. If no error is detected (Routine 84 completion = 'C484') and problem is still suspected or checkout is being performed, go to FSI 31, entry C.

4. If problem has been detected and corrected, remove CE disk from MPL file, replace with customer MPL disk, and perform IMPL operation. Ensure that all controls and cables are returned to normal status. Maintenance procedure complete.

D FSI 31A

5. Re-IMPL and run wraparound microdiagnostics in sequence given:

Routine	Description	Operating Instructions
8C–94	CI Wraparound Tests	MICRO 500, 510
60–6E	Channel Wraparound Tests	MICRO 200, 210

6. If Check 1 Register contents are available, go to FSI 30.

7. If no error is detected and a problem is still suspected, go to device MLM for device checkout and then return here. If no errors are detected, perform a or b below.

Note: *IMPL functional disk before attempting to load from device diagnostic disk at the control module.*

a. If sense bytes are available go to FSI 5.

b. If sense bytes or Check 1 Register contents are not available, perform the following:

(1) Execute IMPL of functional disk.

(2) Ensure that cables, switches, etc., have been returned to normal status.

(3) Customer IPL, if required.

Note: If an error occurs during IPL, turn the Operation Mode switch to Check Stop to freeze the error but only after the completion of the System Reset portion of IPL. A System Reset in Check Stop forces a Check 2 error.

(4) Turn Operation Mode switch to Check Stop.

CAUTION
If an error occurs in check stop mode, it can affect customer operations. Be sure customer agrees before operating in check stop mode.

(5) Run failing program. When an error occurs, go to START 30 and analyze failure.

Note: If dc voltages are marginal or missing, various symptoms can occur. Voltages should be suspect on any intermittent or unusual symptom. See PWR 50 for voltage checks.

8. If problem has been detected and corrected, or checkout was being performed, take action as in step 4.

9. If an EC was installed or installation checkout is being performed, go to entry C, this page.

C

1. 3830 AAA

   a. 3830-2 CE diagnostic disk must be inserted in 23FD and procedures on START 25 completed before this OLT is attempted. Entry B (this page) need not be run.

   b. This OLT should be run when channel failures are suspected, after installation, or after an EC has been installed.

   c. Operating procedures are in the OLT section. Do not attempt to run this OLT without following operating instructions.

2. 3830 AAB

   a. This OLT is used to read the label on any MPL disk inserted in the 23FD. Functional (customer) MPL disk must have successfully executed IMPL before this OLT is attempted.

   b. Run this OLT whenever a new MPL disk is received on an EC or when it is desired to obtain the information (part number, features, etc.) contained in the disk label.

   c. Follow OLT operating procedures in OLT section. 3830 AAB can be run while customer jobs are being executed.

3830-2 | AG0400 Seq 2 of 2 | 4290880 Part No. (2) | 447460 19 Dec 75 | 447461 12 Mar 76 | 447464 15 Nov 77

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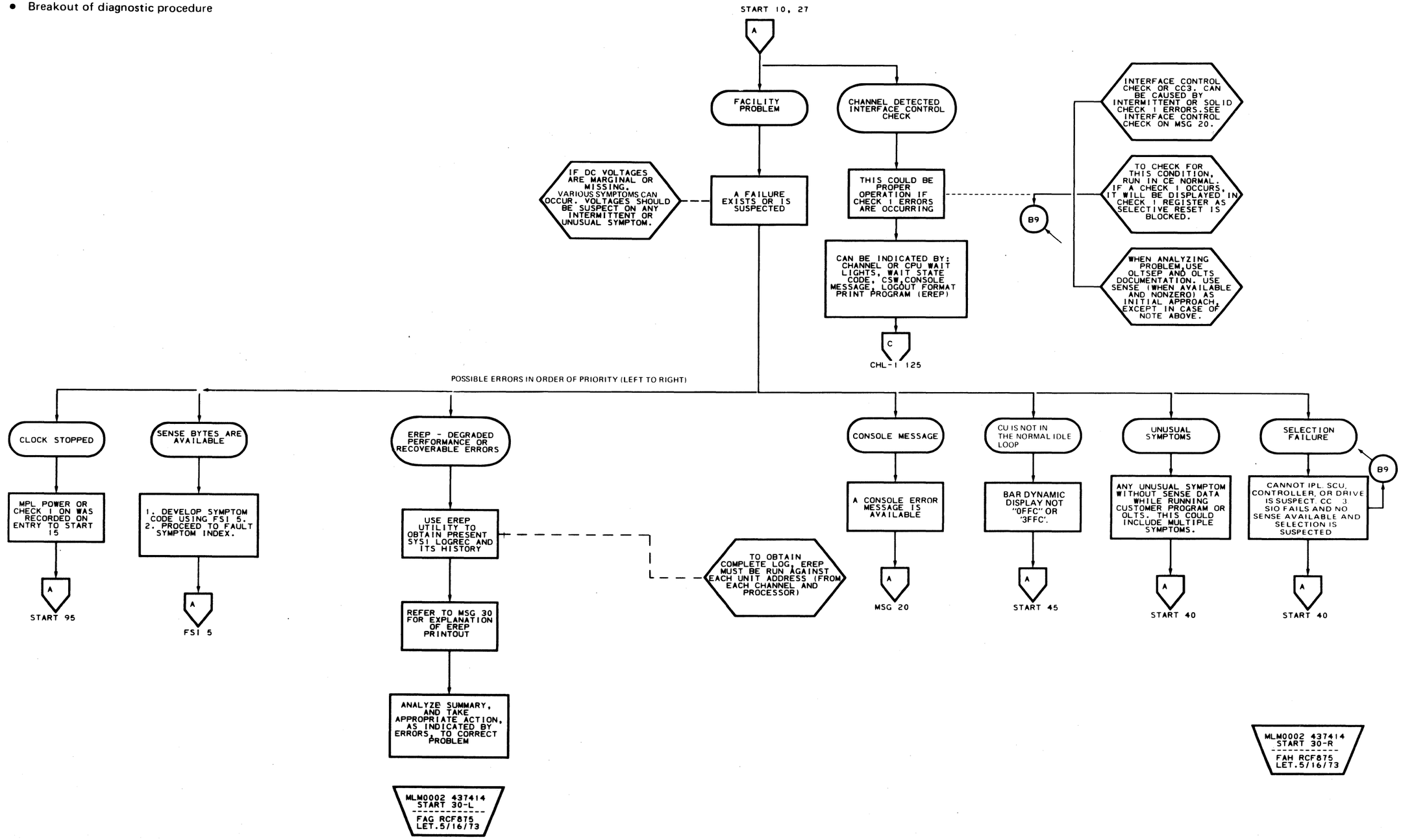
CHECKOUT PROCEDURE (Part 2 of 2) START 27

PROBLEM ANALYSIS

- Breakout of diagnostic procedure



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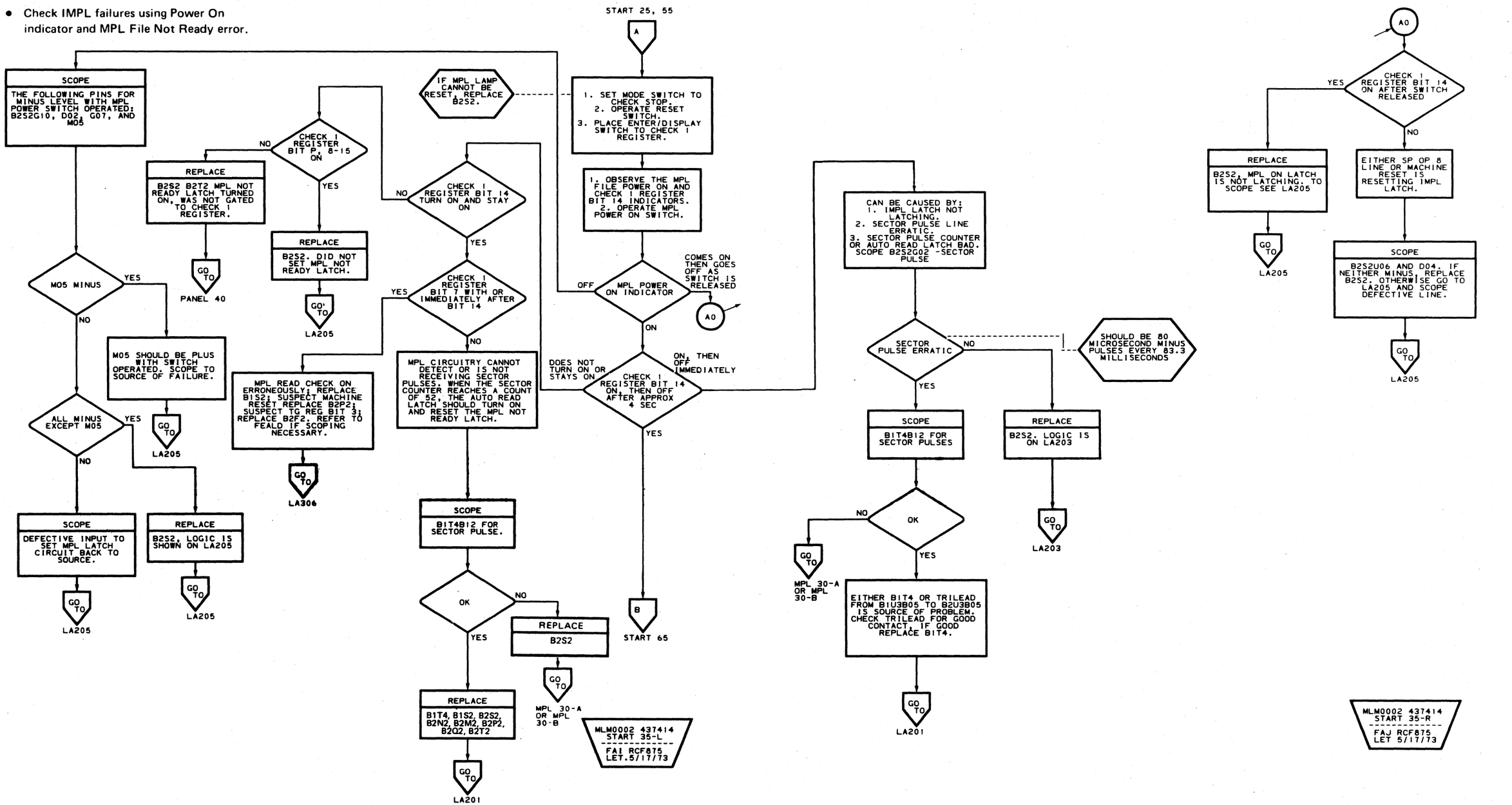
IMPL ANALYSIS

- Check IMPL failures using Power On indicator and MPL File Not Ready error.



AG0500	2346978
Seq. 2 of 2	Part No. (8)

See EC History	437416	437417	447460	447461		
	11 Jan 74	15 Apr 74	19 Dec 75	12 Mar 76		

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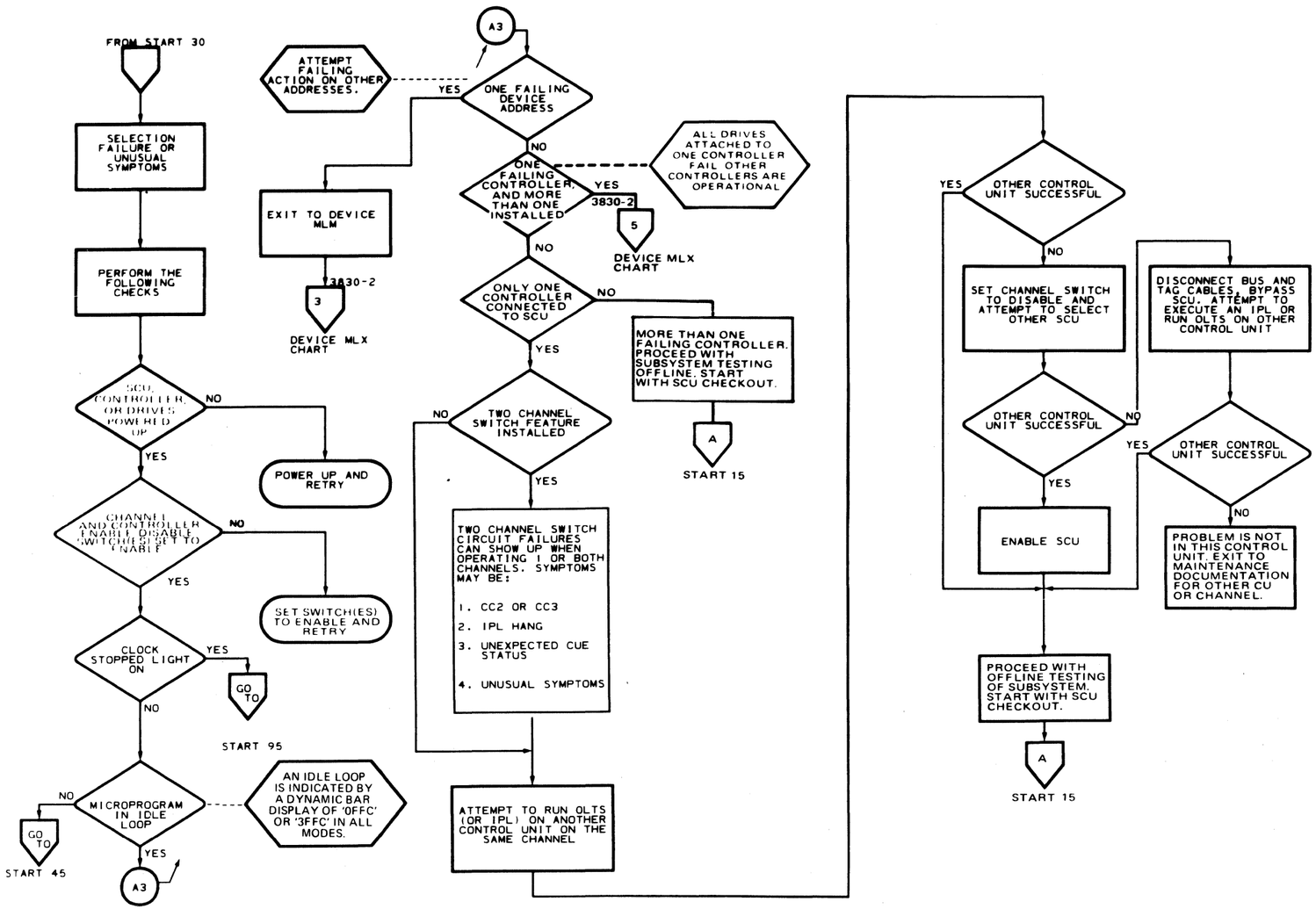
SELECTION FAILURE OR UNUSUAL SYMPTOM



MLM0002 437414
START 40-L
FAK RCF875
LET.5/30/73

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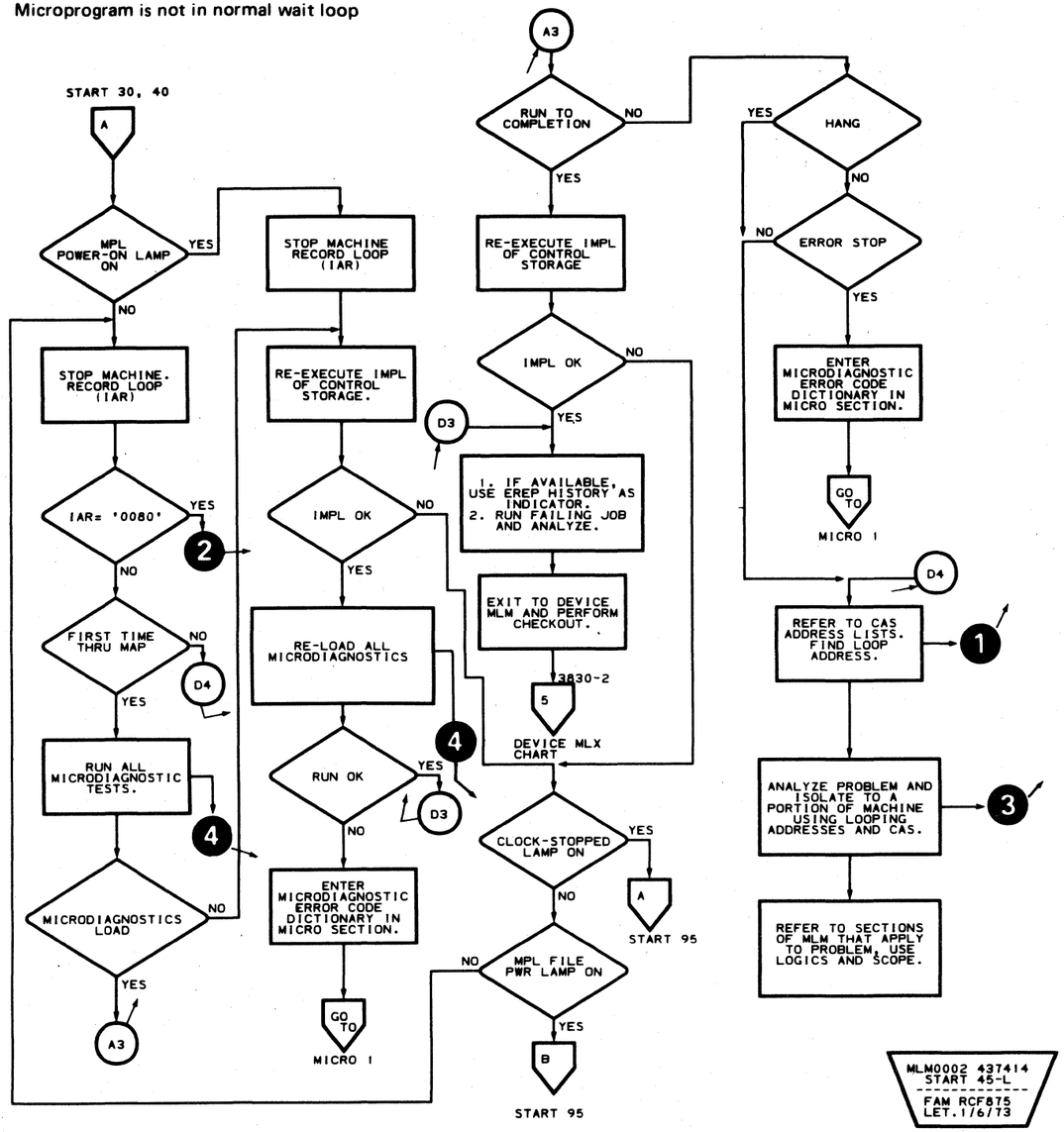
MICROPROGRAM LOOP

- Microprogram is not in normal wait loop



1

Note 1:

1. *If microdiagnostics (other than power-on) are being run and the IAR address is between '0400' and '05FC', a microdiagnostic is looping. To convert the IAR address to the CLD address, subtract '04' from the two high order digits and then add the routine number to the two high order digits. For example: IAR = '0558', subtract '04' to get '0158'. If routine 94 is running, add '94' to get '9558'.*
2. *If the IAR address is between '0000' and '00FC', and the MPL file read head is on tracks zero through seven, the IMPL loader program is looping. To convert the IAR address to the CLD address, replace the two high order digits with '80'.*
3. *All other IAR addresses require no conversion when going to the CLDs.*

When following a loop through CAS, be aware of the registers being gated and their functions. Also be aware of branch conditions such as ST4 or COMMO. Refer to MIC, CTRL, CTL-I portion of MLM. The current microdiagnostic routine loaded is specified in location '0400', byte 0.

2

Note 2:

Address '0080'
If '0680' contains 'F0': contingent connection on unit check
If '0680' does not contain 'F0': contingent connection on stacked status.
Display Byte '0683' - Control Storage

Bits 0-2 = Zero
Bits 3-4 = Controller Address (Binary)
Bits 5-7 = Device Address (Binary)

Bytes '0640' through '0657' contain sense data for unit check error. Contingent connection = CU waiting to present unit check status to channel. Use sense to enter FSI 5 if a drive bit is on in '0680'. Run microdiagnostics in order listed in Note 4. If no help, suspect selection problem; see START 30. (If you came from START 15, return to START 15.)

3

Note 3:

A channel loop is normally indicated by a loop or hang condition in the initial selection, reselection, ending status, or reset portion of CAS. Other areas could cause channel to loop. Suggest observing CPU or channel lights. Analyze CAS loop and run microdiagnostic listed in Note 4. If channel loop is determined, display and record the following registers.

From	Register		Function		To
SCU	MD 0	MD 4	Bus In 0	Bus In 4	Selected Channel
	MD 1	MD 5	Bus In 1	Bus In 5	
	MD 2	MD 6	Bus In 2	Bus In 6	
	MD 3	MD 7	Bus In 3	Bus In 7	
		MD P		Bus In P	
Selected Channel	NA 0	NA 4	Bus Out 0	Bus Out 4	SCU
	NA 1	NA 5	Bus Out 1	Bus Out 5	
	NA 2	NA 6	Bus Out 2	Bus Out 6	
	NA 3	NA 7	Bus Out 3	Bus Out 7	
		NA P		Bus Out P	
SCU	TC 0 TC 1		00 Channel Off 01 Channel Read Control 10 Channel Write Control 11 Channel Freeze Transfer		Channel
	TC 2 TC 3 TC 4 TC 5		Last Byte Request Operation In Address In Status In		
	TC 6 TC 7		00 Not Data Response 01 CTL-I Write 10 CTL-I Read 11 CTL-I Read and S Load		Control Interface
SCU	TB 0 TB 1 TB 2		CTL-I Select Hold CTL-I Tag Gate CTL-I Error Alert Gate		Control Interface
	TB 3 TB 4 TB 5 TB 6 TB 7		Allow Busy Enable CUEND D Enable CUEND C Enable CUEND B Disable CUEND A Allow NA Load		
SCU Not MPL Op	TG 0 TG 1 TG 2 TG 3 TG 4 TG 5 TG 6 TG 7		Unsup Req In Ch B Sup Req In Ch B Unsup Req In Ch A Sup Req In Ch A Block Switch to Ch D Block Switch to Ch C Block Switch to Ch B Block Switch to Ch A		Channel Interface
	TE 0 TE 1 TE 2 TE 3 TE 4 TE 5 TE 6 TE 7		Unsup Req In Ch D Sup Req In Ch D Unsup Req In Ch C Sup Req In Ch C Not Used Not Used Allow Disable Ch C Allow Disable Ch D		

4

Note 4:

Run microdiagnostics in the following order: See MICRO 15 for running instructions
1. *CU: 86, 96, 82, 9A, 98, 84*
2. *CTL-I: 8C-94*
3. *Channel Wraparound: 60-6E*

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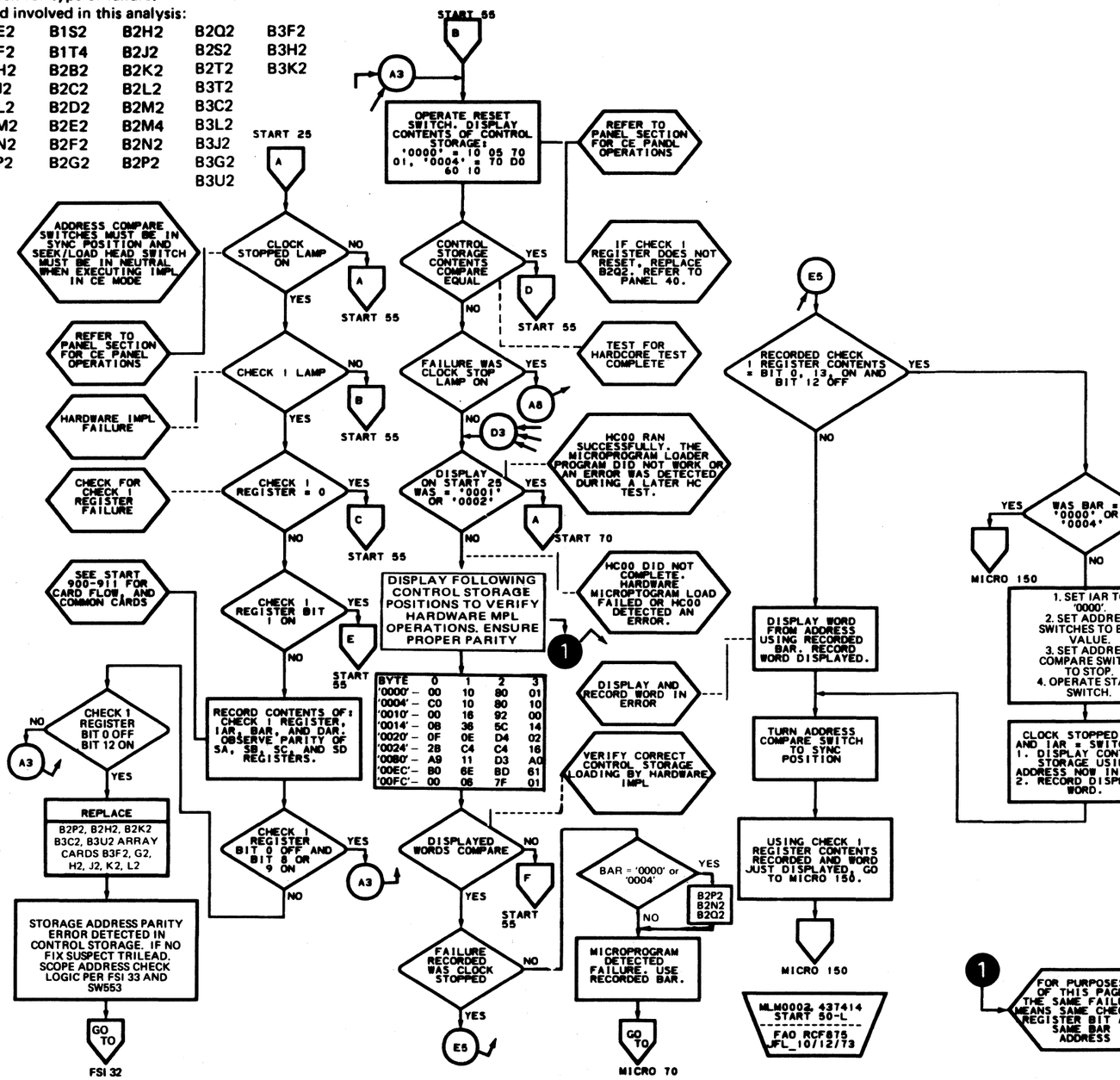
HARDCORE ANALYSIS (Part 1 of 6)

- Check for type of failure.
- Card involved in this analysis:

B1E2	B1S2	B2H2	B2Q2	B3F2
B1F2	B1T4	B2J2	B2S2	B3H2
B1H2	B2B2	B2K2	B2T2	B3K2
B1J2	B2C2	B2L2	B3T2	
B1L2	B2D2	B2M2	B3C2	
B1M2	B2E2	B2M4	B3L2	
B1N2	B2F2	B2N2	B3J2	
B1P2	B2G2	B2P2	B3G2	
			B3U2	



AG0800 Seq. 1 of 2	4290883 Part No. (2)	447460 19 Dec 75	447461 12 Mar 76				

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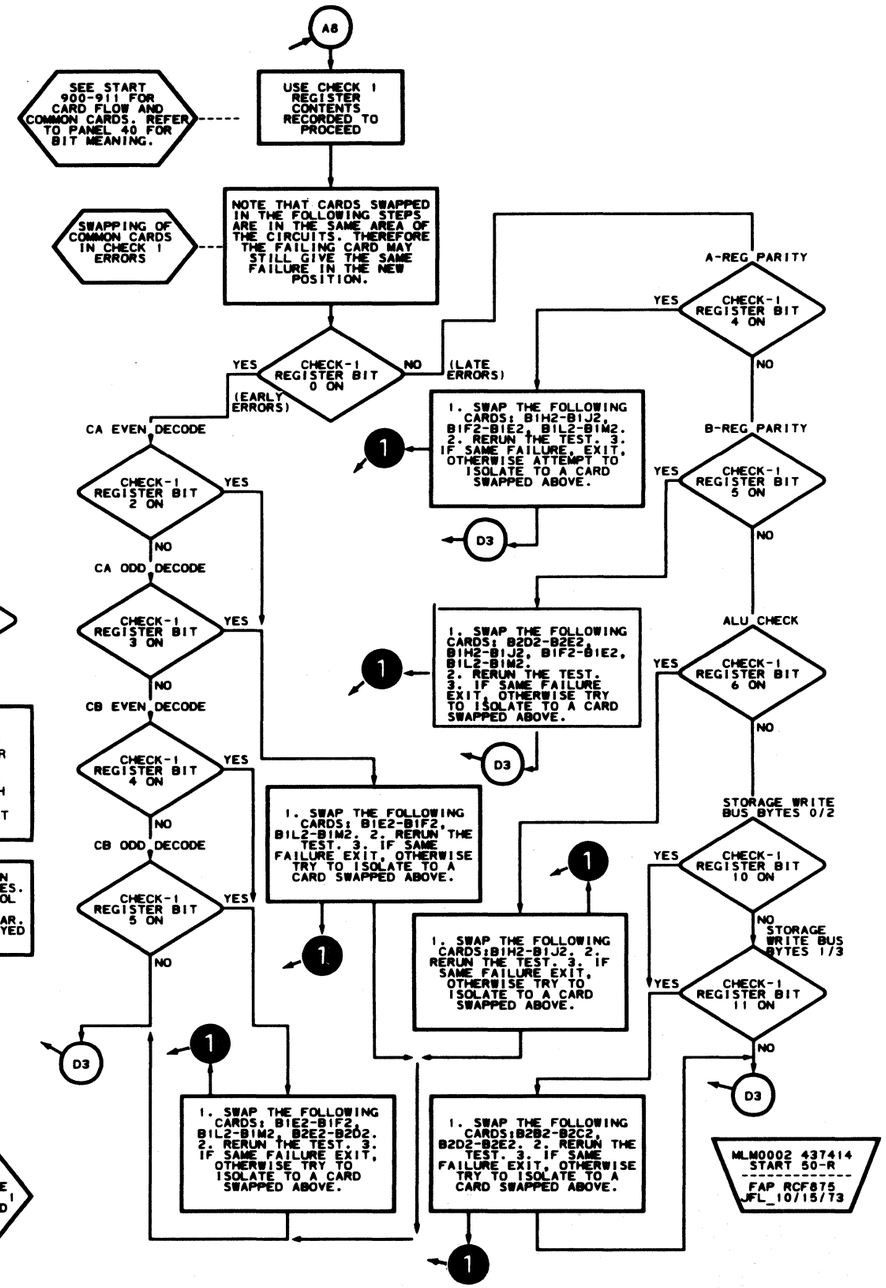
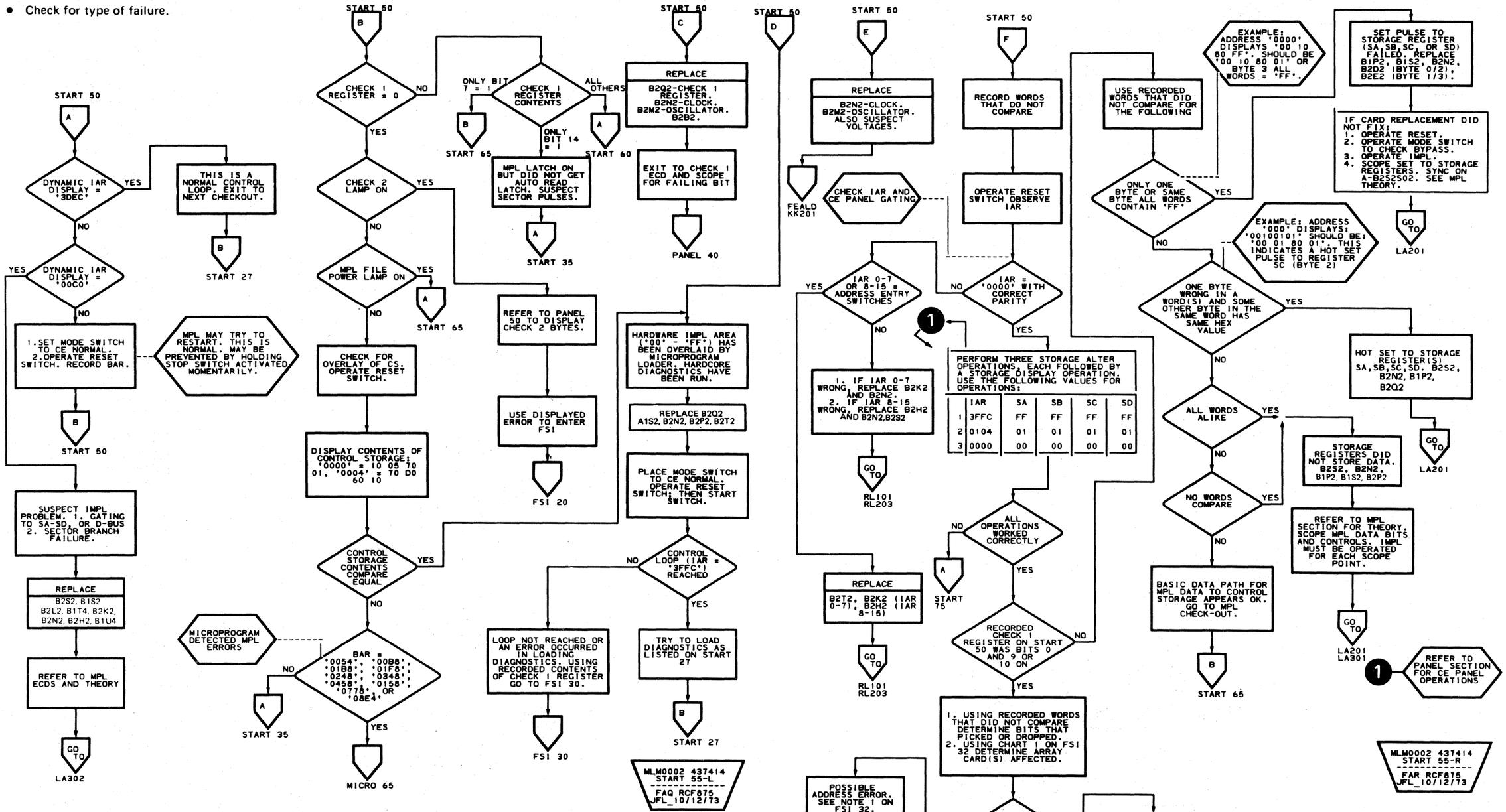


HARDCORE ANALYSIS (Part 2 of 6)

- Check for type of failure.



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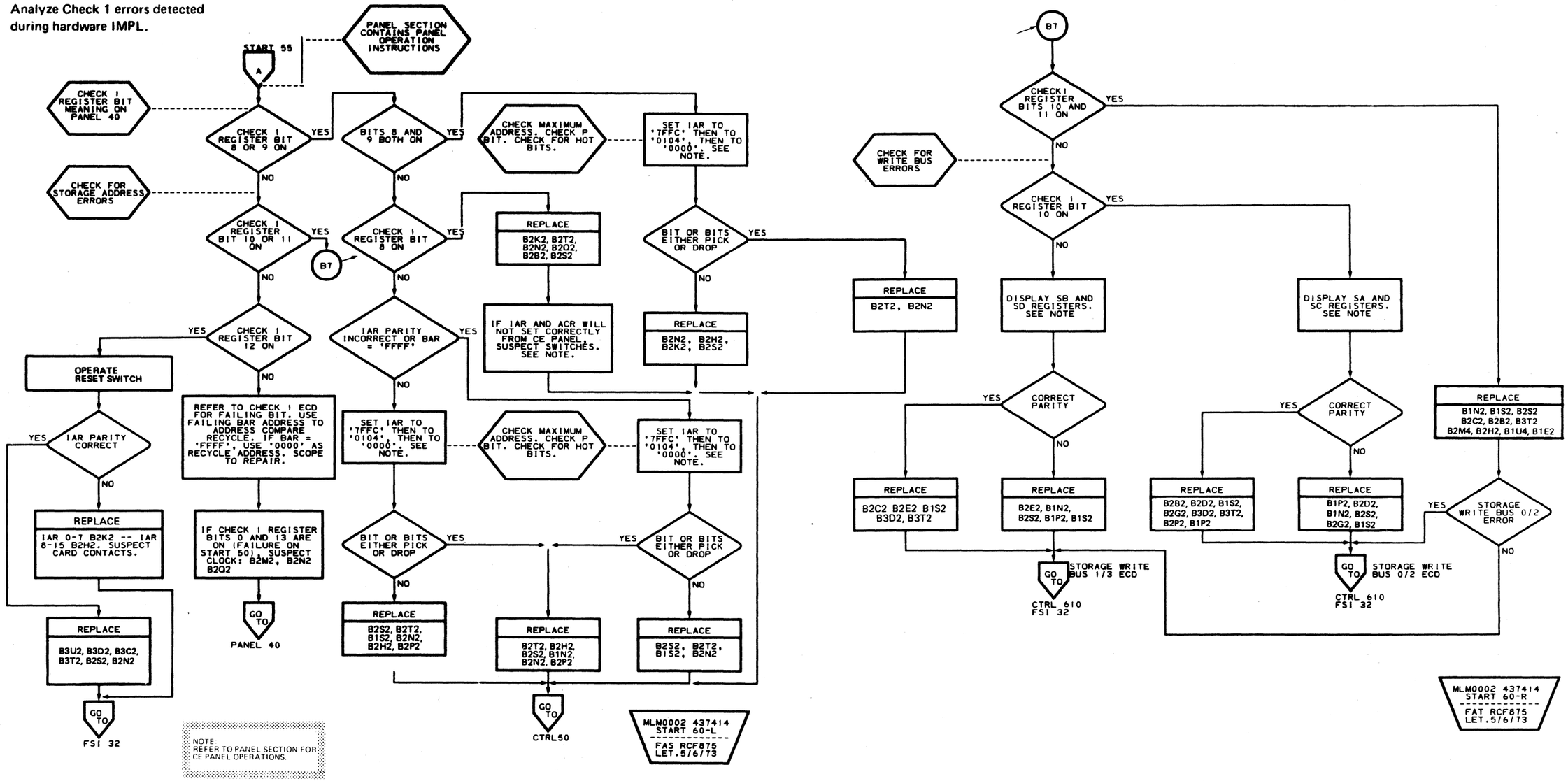
HARDCORE ANALYSIS (Part 3 of 6)

- Analyze Check 1 errors detected during hardware IMPL.



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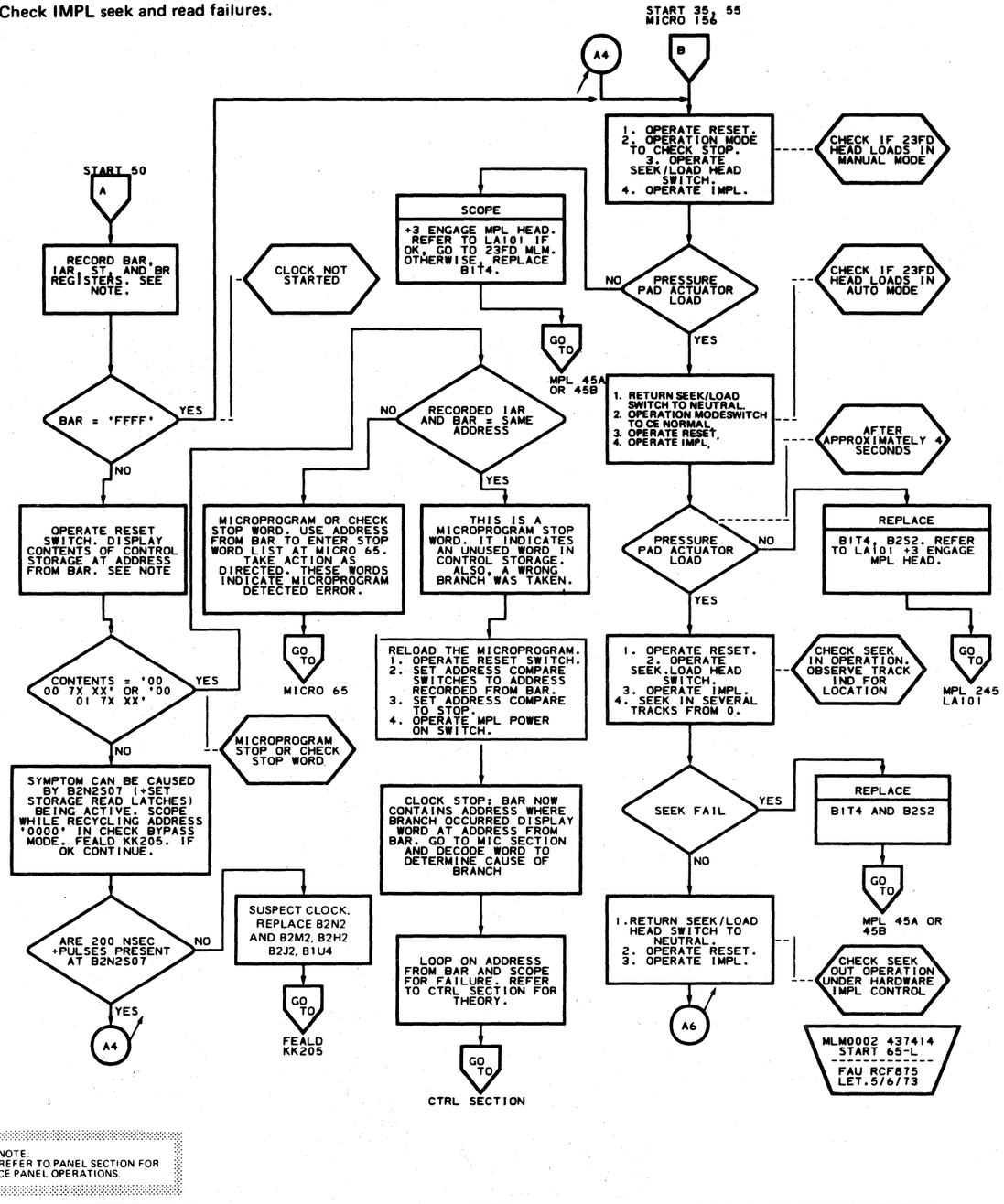
HARDCORE ANALYSIS (Part 4 of 6)

- Check IMPL seek and read failures.



NOTE
REFER TO PANEL SECTION FOR CE PANEL OPERATIONS.

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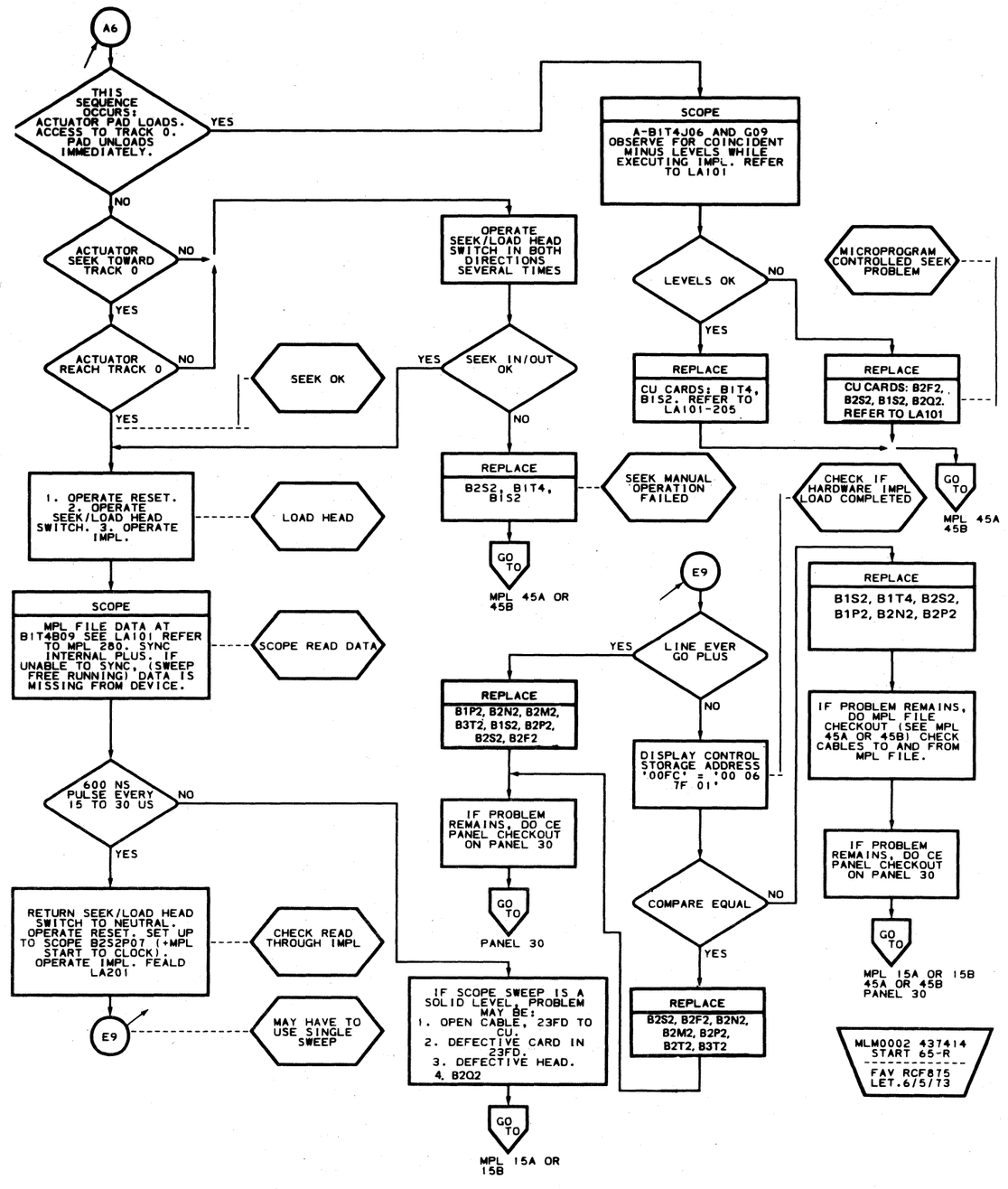
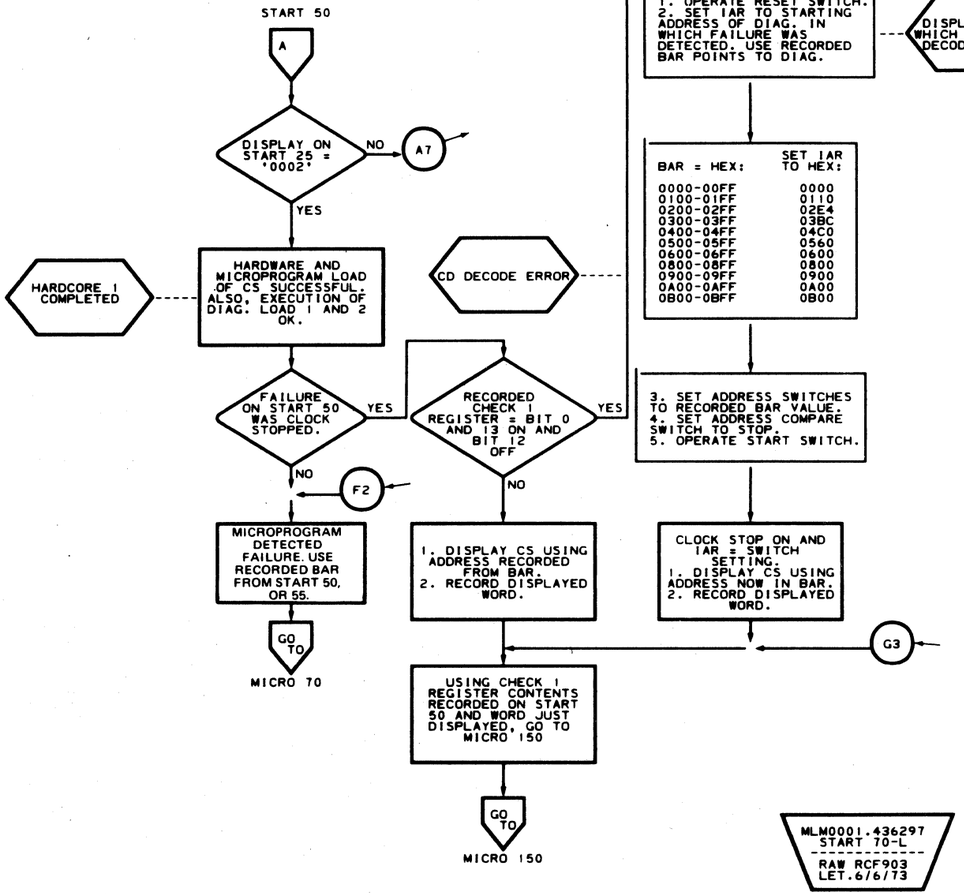
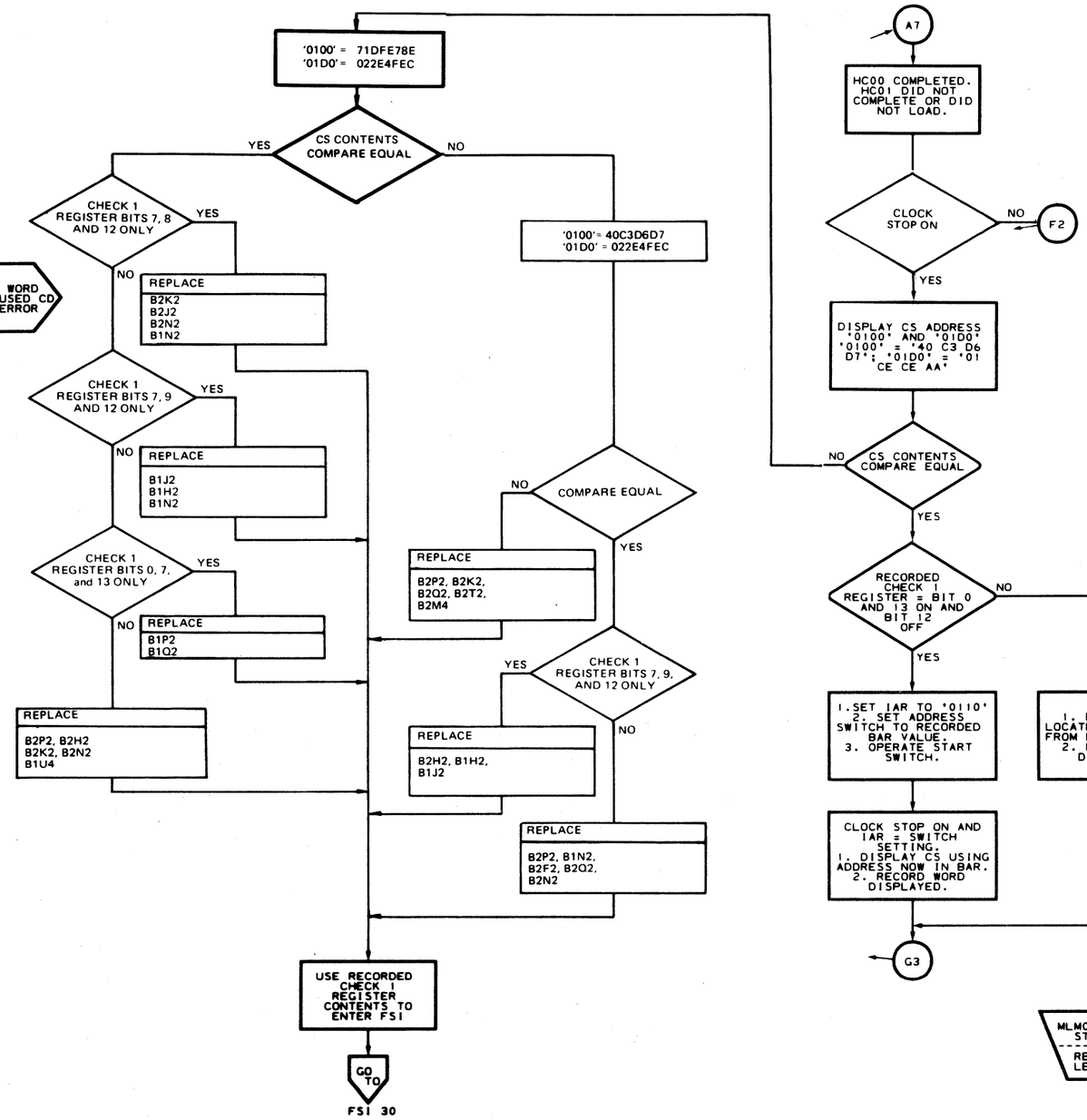
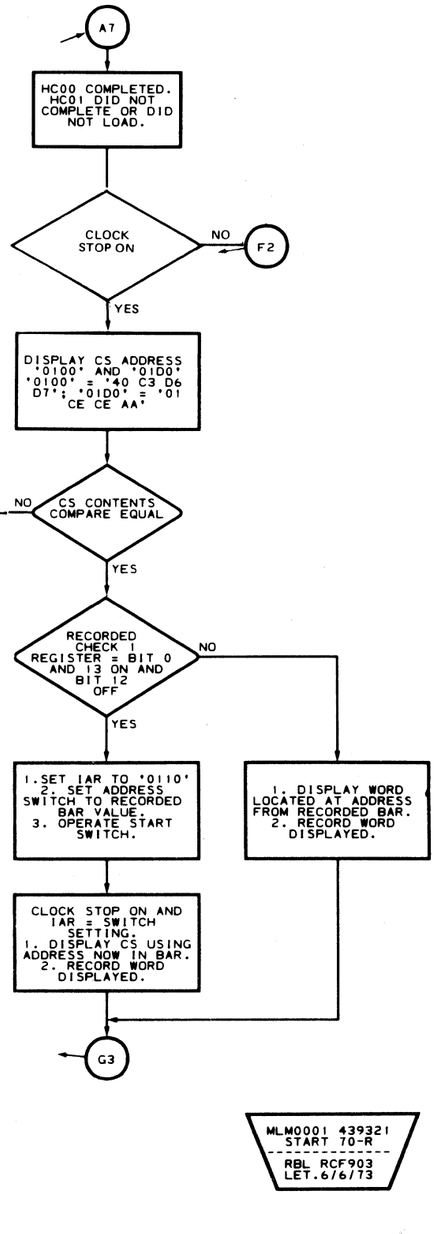


HARDCORE ANALYSIS (Part 5 of 6)

- Check if hardcore test 1 loaded and ran correctly.







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- Check for failure in the data path, address path, or control storage during a manual operation.

START 55 (A) / MICRC 420 (B)

SAME BYTE FAILS — NO / YES

1. SET DISPLAY SWITCH TO REGISTER SELECT
2. SET REGISTER SELECT TO FAILING BYTE
   BYTE 0 SA REGISTER
   BYTE 1 SB REGISTER
   BYTE 2 SC REGISTER
   BYTE 3 SD REGISTER
3. OBSERVE REGISTER DISPLAY LIGHTS WHILE ROTATING DATA ENTRY SWITCHES.

DISPLAY LIGHTS FOLLOW SWITCHES — NO / YES

HOT SET LINE TO REGISTER REPLACE B1P2

GO TO DE 103

GO TO PANEL 30

STORAGE REGISTER SET CORRECTLY (SA,SB,SC,SD) — NO / YES — REFER TO PANEL SECTION FOR CE PANEL OPERATIONS

IAR SET CORRECTLY — NO / YES

STORAGE DISPLAYED CORRECTLY — NO / YES

RETURN TO START 55 AND VERIFY THAT PROCEDURES WERE CORRECTLY FOLLOWED TO THIS POINT. IF THESE WERE FOLLOWED, PROCEED TO CE PANEL CHECKOUT. SUSPECT;
1. CLOCK AND ITS START/STOP CONTROLS.
2. CE PANEL SWITCHES.
3. VOLTAGES.

ALL BYTES DISPLAYED = 'FF' — YES / NO

STORAGE READ/WRITE NOT CORRECT OR MACHINE RESET ACTIVE. 1. SUSPECT CARDS B3C2, B1P2, B2N2, AND B2P2. 2. SUSPECT TRILEAD.

GO TO SW4XX SW5XX

CTRL 600-610 (THEORY)

1. MATCH THE FOLLOWING SUSPECT CARDS WITH FAILURE INDICATION:

BYTE 0 B3T2, B3C2, B2K2, B2G2 ARRAY CARDS B3G2, B3J2, B3L2
BYTE 1 B3T2, B3C2, B2J2 ARRAY CARDS B3F2, B3H2, B3K2
BYTE 2 B3T2, B3C2, B2H2 ARRAY CARDS B3F2, B3H2, B3K2
BYTE 3 B3T2, B3C2, B2L2 ARRAY CARDS B3G2, B3J2, B3L2
ALL BYTES B3C2,B3T2,B2N2,B2G2

SUSPECT TRILEADS
CHECK B3 BOARD VOLTAGES

2. SCOPE FOR FAILURE USING STORAGE ALTER/DISPLAY AND FAILING PATTERN. REFER TO PANEL 115 AND CTRL 600.

GO TO FSI 32

NOTE: SIMPLIFIED STORAGE ALTER DISPLAY DIAGRAM IS ON PANEL 115.

SET ACR WITH SAME PATTERNS USED TO SET IAR

ACR FAIL — YES / NO

IAR BYTE(S) FAILING — 0 AND 1 / 0 / 1

SUSPECT CARDS B2T2, B2N2 AND B2S2 — GO TO KP101-103

SUSPECT CARDS B2K2, B2B2, B2T2, AND B2N2 — GO TO KP101

SUSPECT CARDS B2H2, B2C2, B2T2, AND B2N2 — GO TO KP103

WHICH BYTE(S) — 0 AND 1 / 0 / 1

1. SUSPECT CARDS: B2T2, B2P2
2. SUSPECT ACR SWITCHES
GO TO KP105

1. SUSPECT CARDS: B2B2 B2T2, AND B2P2
2. SUSPECT ACR SWITCHES
GO TO RL305

1. SUSPECT CARDS: B2C2 B2T2, AND B2P2
2. SUSPECT ACR SWITCHES
GO TO RL405

MLM0002 437414 START 75-L
FAY RCF875 LET.6/6/73

WHICH REGISTER FAILED — SA, SB, SC, AND SD / SA OR SC / SB OR SD

1. SWAP B2E2 (SB, SD) WITH B2D2 (SA, SC). 2. SET FAILING REGISTER (SB OR SD) WITH FAILING VALUE. 3. IF REGISTER SETS OK, REPLACE CARD NOW IN B2D2; OTHERWISE, CONTINUE.

1. SWAP B2D2 (SA, SC) WITH B2E2 (SB, SD). 2. SET FAILING REGISTER WITH FAILING VALUE. 3. IF REGISTER SETS OK, REPLACE CARD NOW IN B2E2; OTHERWISE, CONTINUE.

REGISTER VALUE CHANGES WHEN SET ATTEMPTED — YES / NO

SUSPECT SET OR GATE PULSES

SUSPECT CARDS: B2N2, B2T2, B2G2, AND B2S2 OR SCOPE LOGIC STARTING ON RS302 (B BUS) WHILE ATTEMPTING TO SET REGISTER

GO TO RS302

GO TO START 80 AND PERFORM MANUAL REGISTERS TEST

A

START 80

MLM0002 437414 START 75-R
FAZ RCF875 LET.6/6/73

AG1000 Seq. 2 of 2	4290885 Part No. (2)	447460 19 Dec 75	447461 12 Mar 76				

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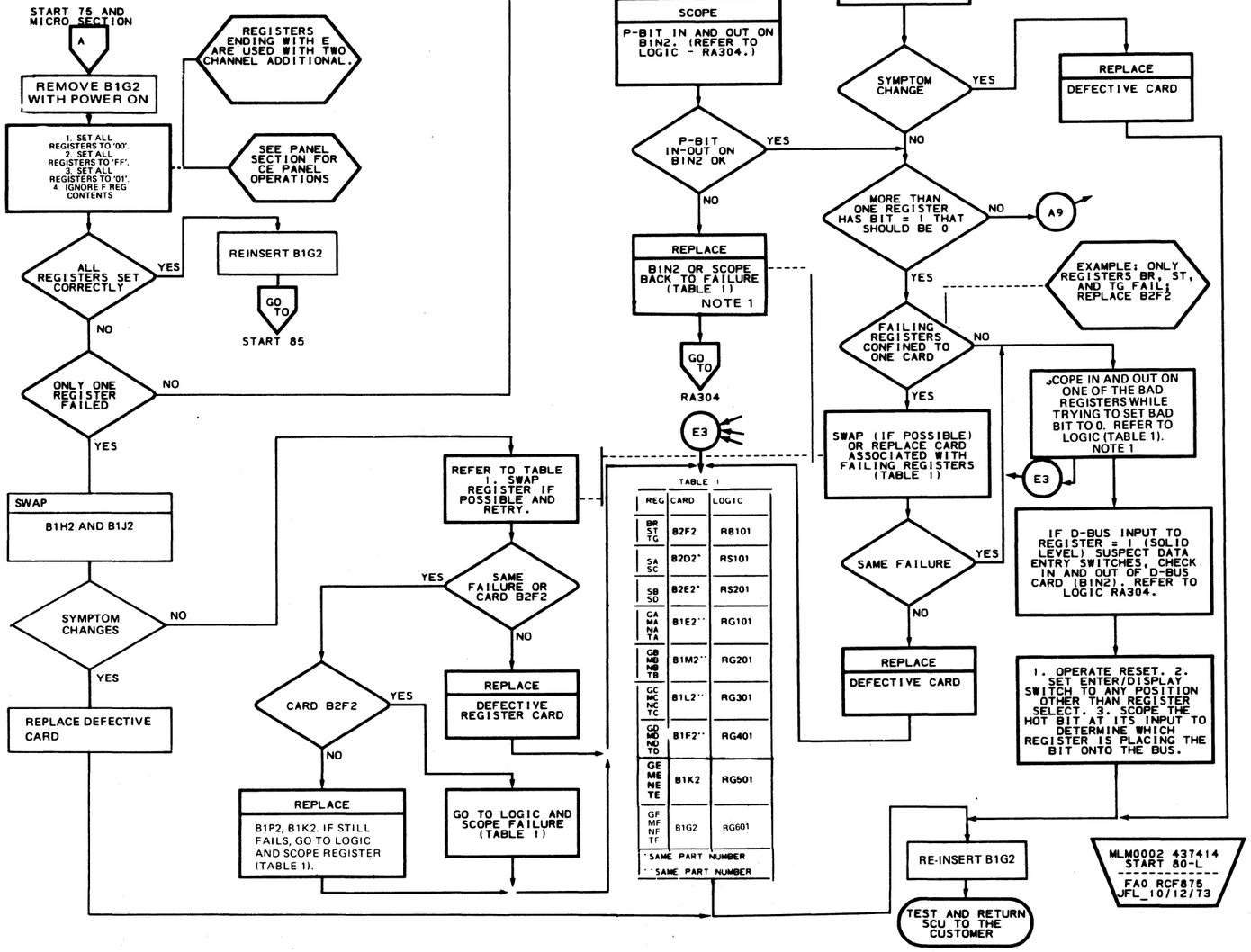
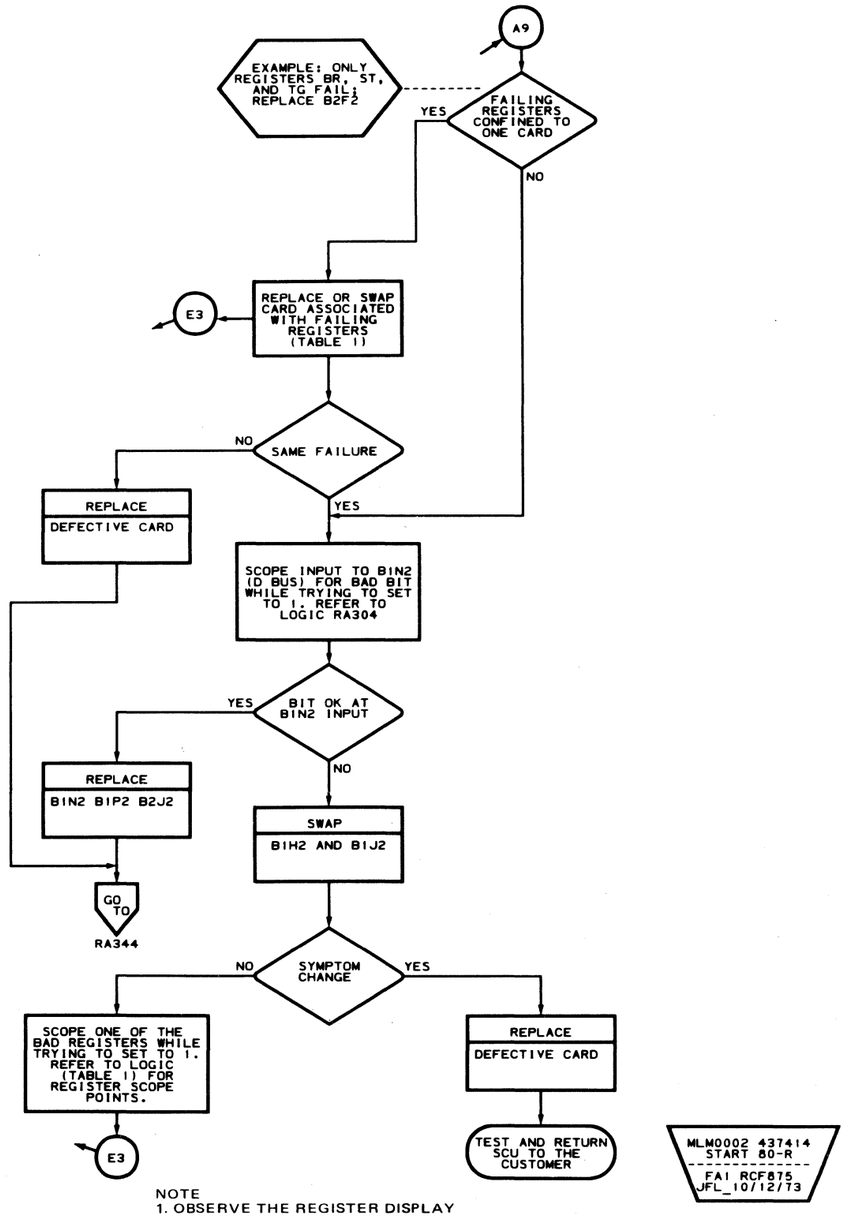
MANUAL REGISTERS TEST (Part 1 of 2)

- Test general purpose register by manual set/reset of bit patterns.
- Cards involved in this analysis:

B1E2	B1K2	B1P2
B1F2	B1L2	B2D2
B1G2	B1M2	B2E2
B1H2	B1N2	B2F2
B1J2		B2J2





NOTE
1. OBSERVE THE REGISTER DISPLAY LIGHTS AND PULL THE REGISTER CARDS ONE AT A TIME. IF THE CARD CAUSING THE HOT BIT IS PULLED THE BIT LIGHT MAY GO OFF. THIS MAY INDICATE THE DEFECTIVE REGISTER CARD.

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MANUAL REGISTERS TEST (Part 2 of 2)

- Use a microprogram word to test the A- and B-registers.
- Cards involved in this analysis:

A1N2	B1E2	B1J2	B1M2	B1Q2	B2E2	B2H2	B2L2
A1T2	B1F2	B1K2	B1N2	B1R2	B2F2	B2J2	B2N2
B1D2	B1H2	B1L2	B1P2	B2D2	B2G2	B2K2	B1G2

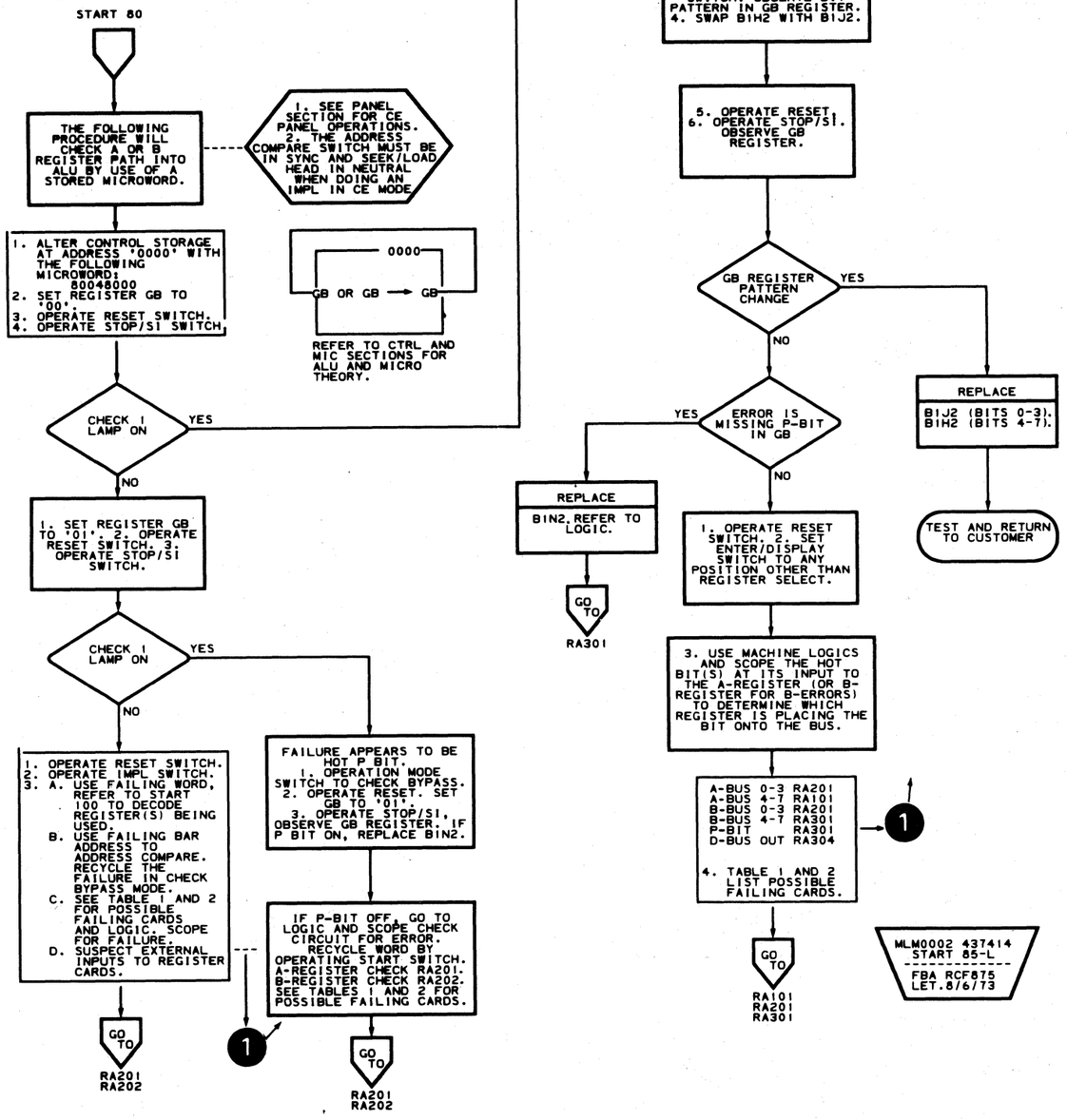


Table 1. A-Register

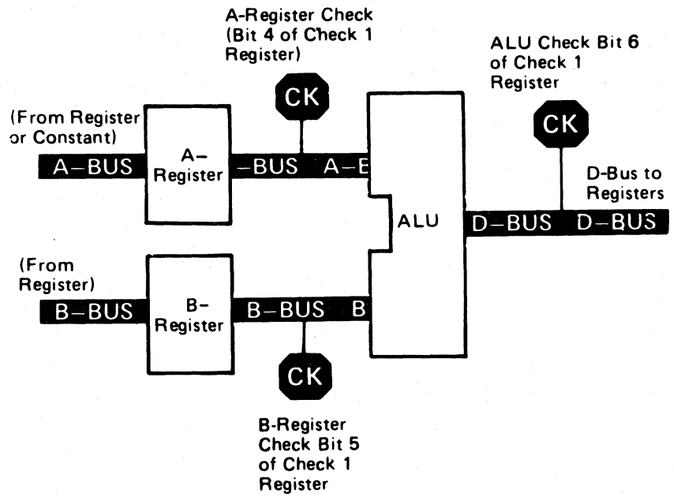
Register	Card	External Input	Logic
GC	B1L2		RG301 – 306
NC			
TC		B2H2	
MC		B2K2	
MD	B1F2		RG401 – 406
TD		B1J2, B1H2	
ND		B1R2,B1Q2,B1N2	
GB	B1M2	B2K2	RG201 – 206
NB			
TB			
MB		B1Q2	
GA	B1E2	B1Q2	RG101 – 106
NA		A1T2, B1N2	
TA		B1J2	
MA		B1D2, B1F2	
ALU 0 – 3	B1J2		RA201 – 203
ALU 4 – 7	B1H2		RA101 – 103
ALU P	B1N2		RA301 – 304
Clock	B2N2		KK201 – 205
CD Decode, Reg Sets	B1P2 B2H2	B2K2	DE101 – 106
IAR, DAR, CK Format Decode	B2H2 B1N2	B2K2, B1H2	RL101 – 105
IAR, DAR, TAR, CA Decode, Format Decode	B2K2 R1H2		RL201 – 207

1

Table 2. B-Register

Register	Card	External Input	Logic
GC	B1L2		RG301 – 306
NC			
TC			
MC			
GD	B1F2		RG401 – 406
ND		B1R2, B1Q2	
TD			
MD			
GB	B1M2		RG201 – 206
NB			
TB			
MB		B1Q2	
GA	B1E2		RG101 – 106
NA		A1T2	
TA		B1Q2	
MA		B1D2, B1N2	
GE	B1K2		RG501
NE			
TE			
ME			
TF	B1G2	B1U4	RG601
GF			
MF			
NF			
SA	B2D2	B2G2, B2H2, B2J2, B2K2, B2L2, B1E2, A1N2	RS101 – 103
SC		A1N2, B1E2, B2H2	
SB	B2E2	B2J2, A1N2, B1E2	RS201 – 203
SD		B1N2, B1E2, B2L2	
BR	B2F2		RB101 – 106
ST			
TG			
ALU 0 – 3	B1J2		RA201 – 203
ALU 4 – 7	B1H2		RA101 – 103
ALU P	B1N2		RA301 – 304
Clock	B2N2		KK201 – 205
CD Decode, Reg Sets	B1P2	B1N2, B2J2	DE101 – 106
IAR, DAR, Format Decode	B2H2		RL101 – 105
IAR, DAR, TAR, CA Decode, Format Decode	B2K2		RL201 – 207

REFER TO START 900-911 FOR CARD FLOW AND COMMON



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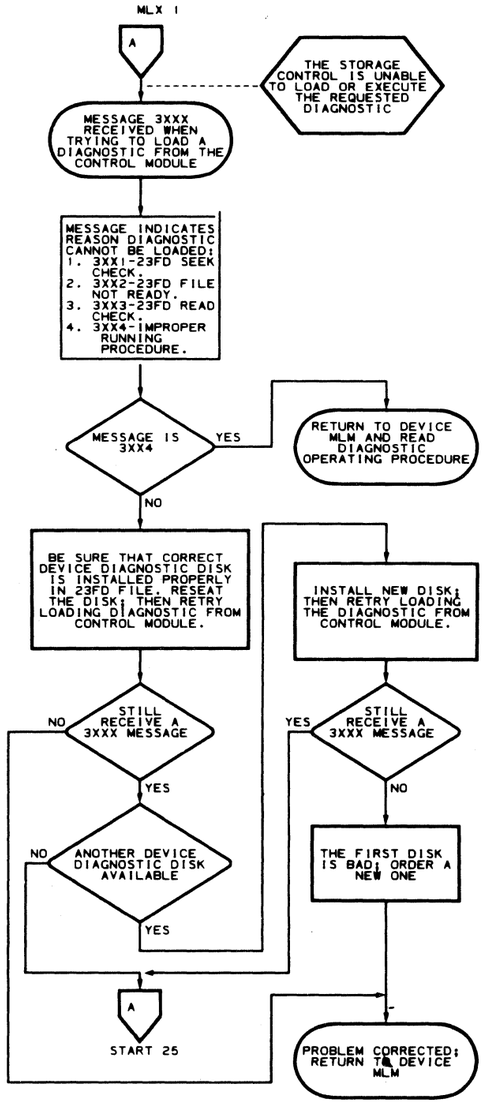

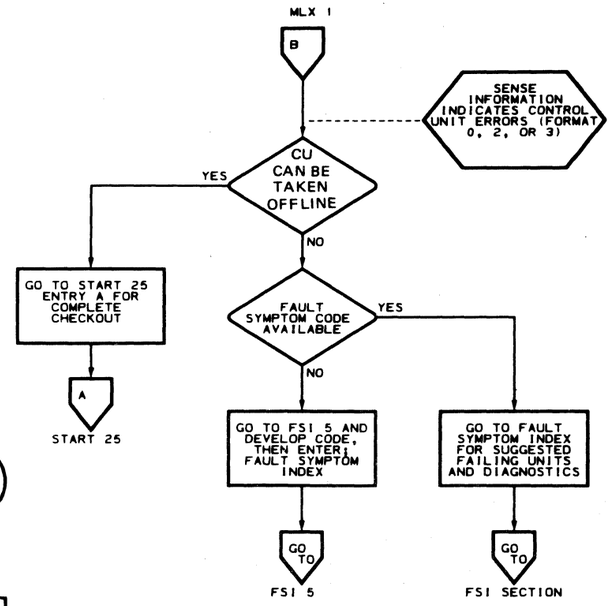

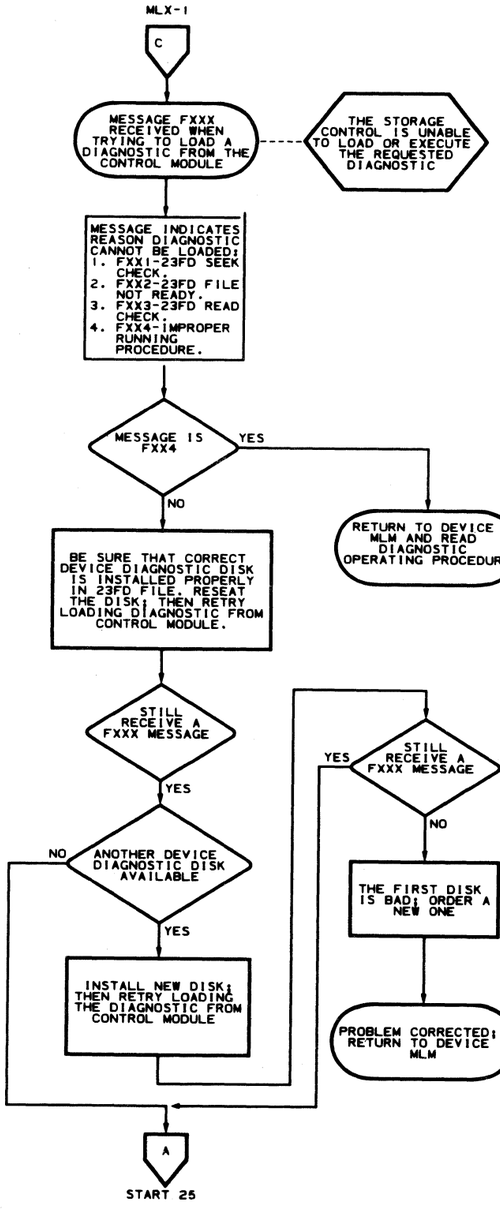

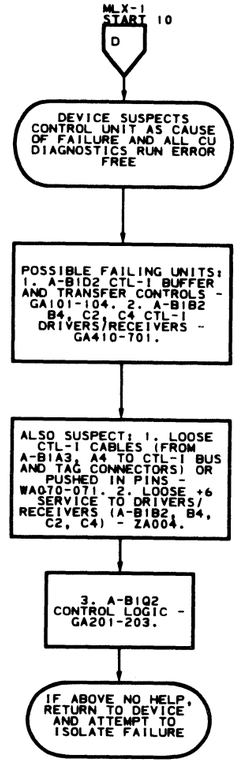

MLM0002 437414
START 90-L
FA2 RCF875
JFL_10/12/73

MLM0002 437414
START 90-R
FA3 RCF875
JFL_10/12/73

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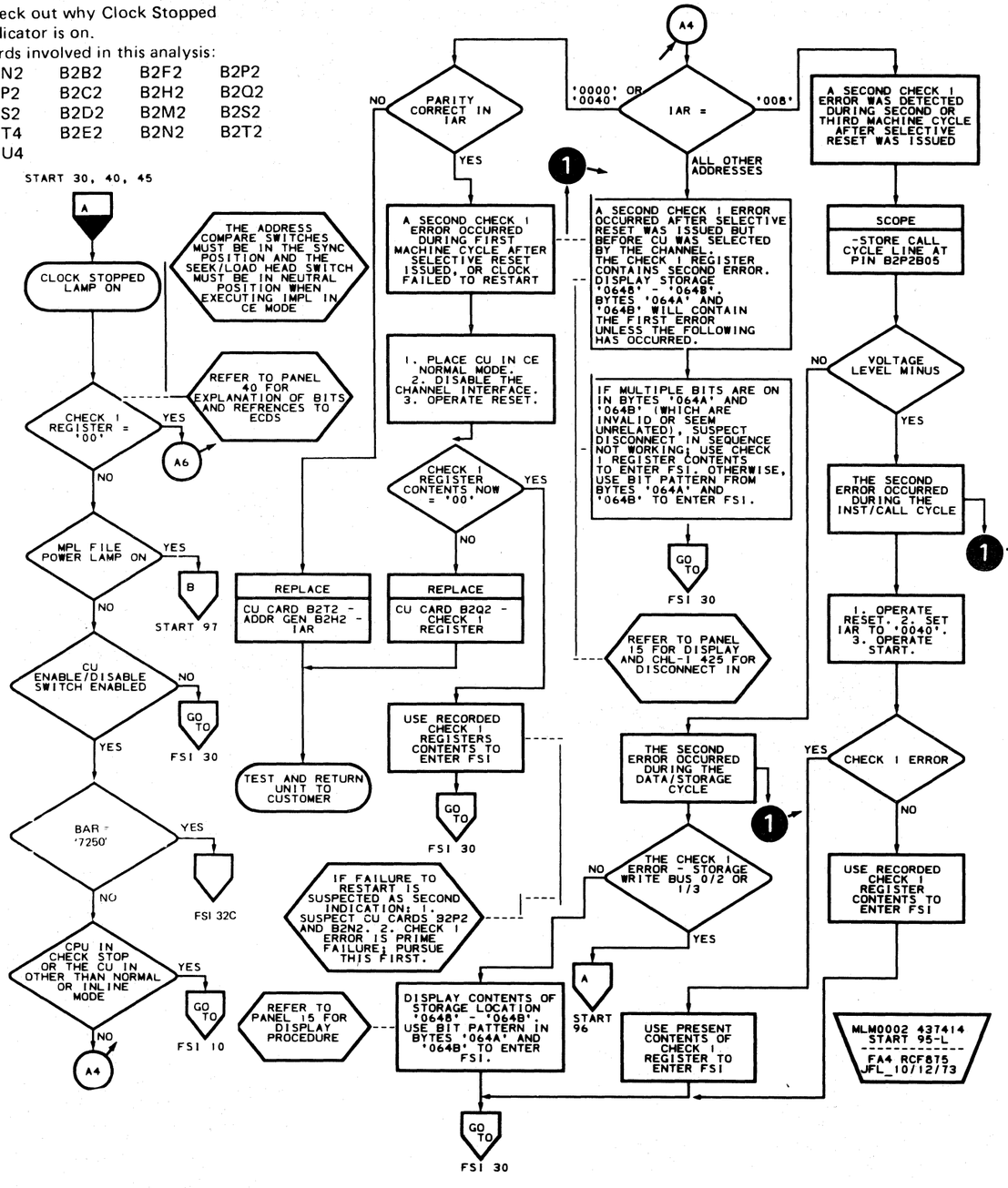
CU CLOCK STOPPED ANALYSIS (Part 1 of 3)

- Check out why Clock Stopped indicator is on.
- Cards involved in this analysis:

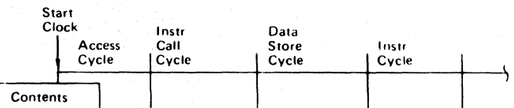
B1N2	B2B2	B2F2	B2P2
B1P2	B2C2	B2H2	B2Q2
B1S2	B2D2	B2M2	B2S2
B1T4	B2E2	B2N2	B2T2
B1U4			



1

Storage Location

'0648'	'0649'	'064A'	'064B'
Backup Addr Reg		Check 1 Reg	
0 7	8 13	0 7	8 15



Contents with clock Stopped				
IAR =	'0040'	'0008'	'0008'	'000C'
BAR =	1st Fail Addr	1st Fail Addr	1st Fail Addr	'0008'
DAR =				
CHK-1 REG =	1st Error	1st Error	2nd Error	2nd Error

MLM0002 436397
START 95-R
FA5 RCF875
JFL_10/12/73

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CU CLOCK STOPPED ANALYSIS (Part 2 of 3)

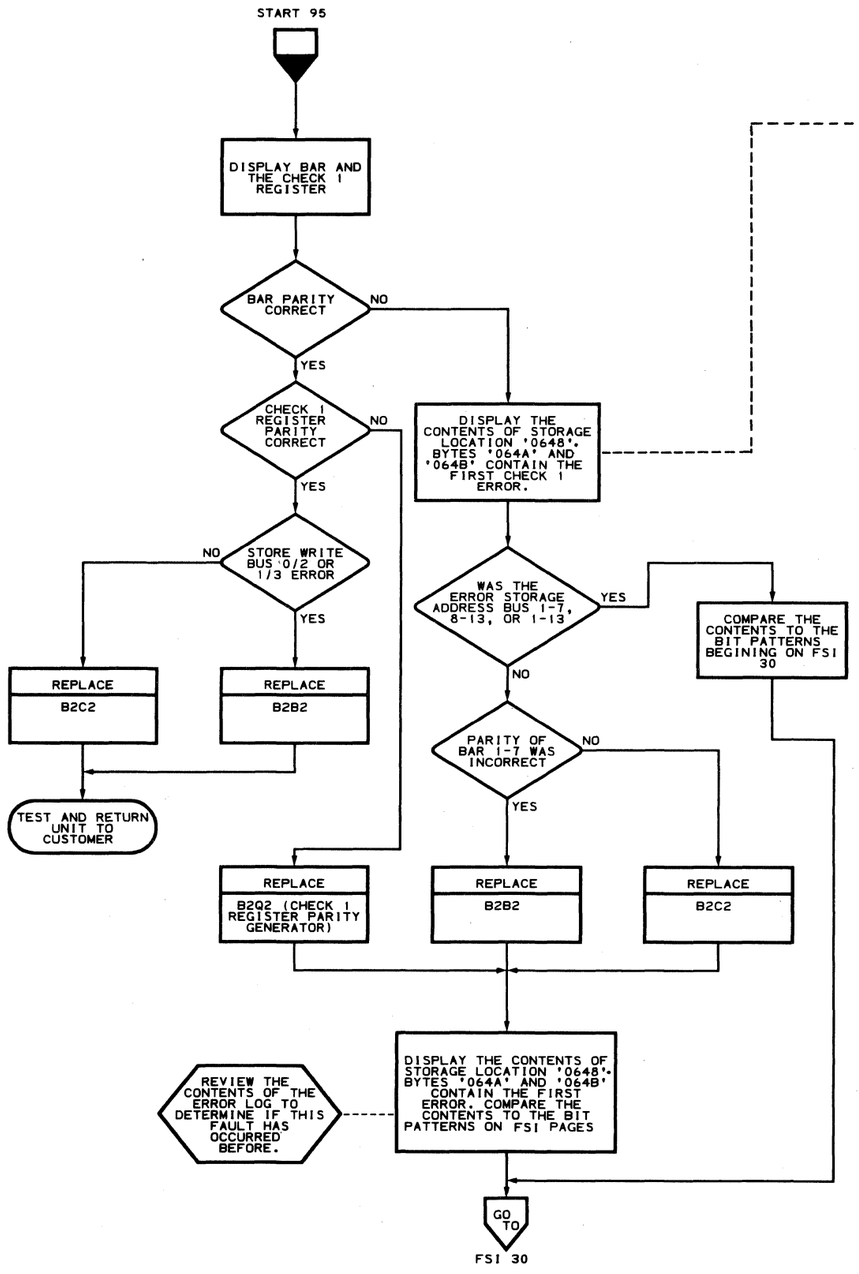
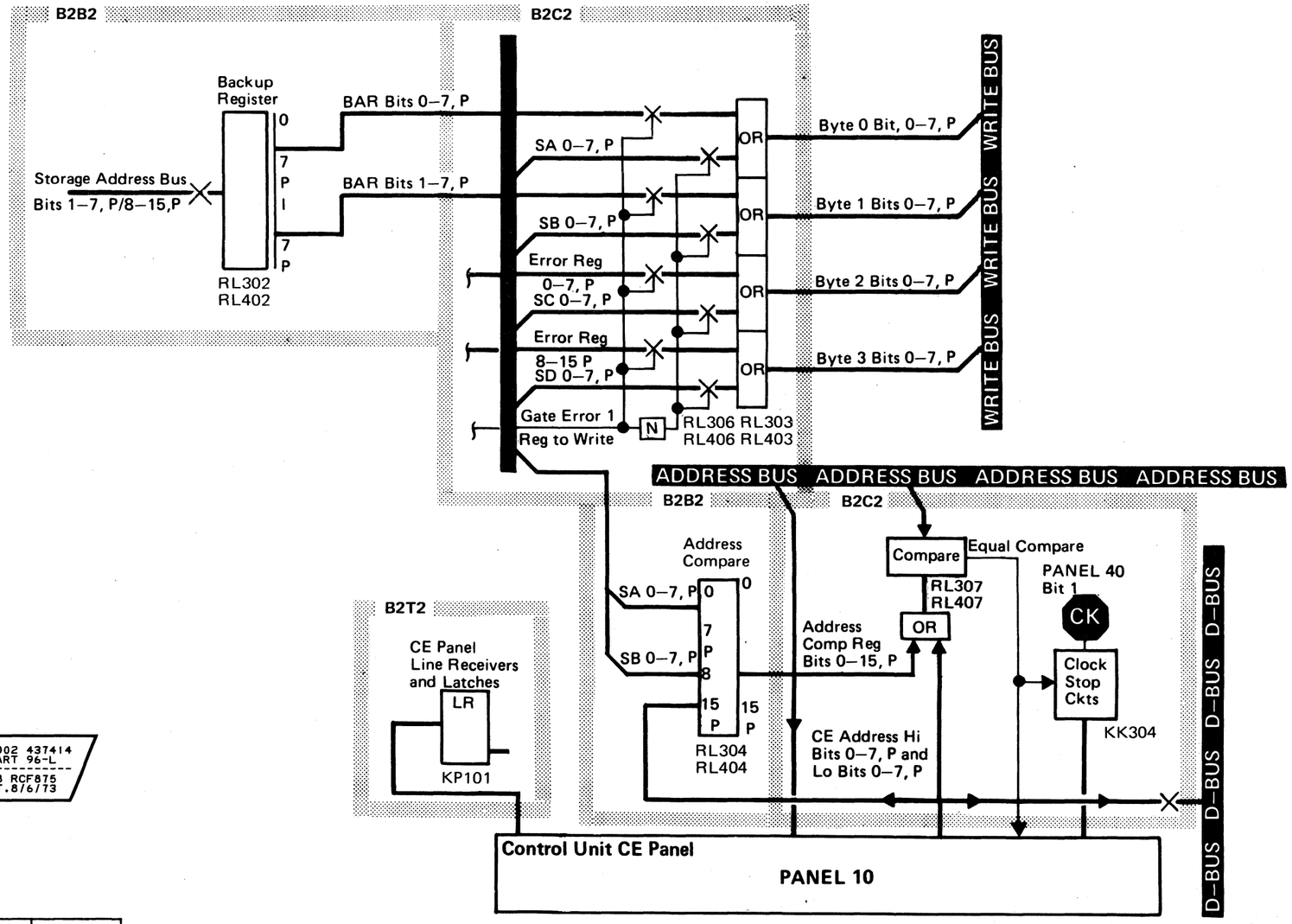


Chart 1
Storage Location '0648'

'0648'		'0649'	'064A'		'064B'
Back-up Addr Reg			Check-1 Reg		
0	7 | 8	13	0	7 | 8	15



AG1300	2347338	437403	437404	437405	437408	437413	437414	
Seq. 1 of 2	Part No.( )	21 Apr 72	23 Jun 72	15 Aug 72	16 Oct 72	5 Mar 73	4 Jun 73	

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CU CLOCK STOPPED ANALYSIS (PART 3 OF 3)

START 97

START 95

B

CHECK 1 REGISTER CONTENTS

ONLY BIT 14 = 1

FILE NOT READY MPL 30

ONLY BIT 7 = 1

FILE READ CHECK

ALL OTHER BIT COMBINATIONS

CHECK 1 LAMP ON

NO

YES

TURN DC POWER OFF; THEN TURN DC POWER ON. CONTROL STORAGE CONTAINS RANDOM DATA AND PARITY.

STORAGE INTEGRITY MUST BE VERIFIED BEFORE CHECK 1 ERRORS ARE CONSIDERED VALID.

1. RECORD CHECK 1 REGISTER CONTENTS BEFORE RESETTING.
2. OPERATE RESET.

DISPLAY THE CONTENTS OF THE FOLLOWING STORAGE LOCATIONS. THE CONTENTS SHOULD BE:

HEX ADDRESS	BYTE 0	1	2	3
0000	10	73	D0	01
0004	62	C4	D2	11
0008	92	61	D6	10
000C	20	61	C6	10

B2

B2

ALL LOCATIONS DISPLAYED CORRECT

NO

YES

CHECK CU AND MPL VOLTAGES. IF OK, PROCEED

USING CHECK 1 REGISTER CONTENTS TO ENTER FSI COMPARE BIT PATTERNS ON SYMPTOM INDEX PAGES

GO TO

FSI 30

REPAIR TEST AND RETURN SCU TO CUSTOMER

ONLY A FEW WORDS ARE USED FOR QUICK VERIFICATION. FOR DETAILED EXAMINATION, REFER TO CLDS AND MPL SECTION.

MLM0002 437414
START 97-L
FA6 RCF875
LET. 8/7/73

START 95

C

A4

PLACE CU IN CHECK STOP. OPERATE SEEK/LOAD HEAD SWITCH

PRESSURE PAD ACTUATOR LOAD

NO

YES

MPL 45A OR 45B

THE ADDRESS COMPARE SWITCHES MUST BE IN THE SYNC POSITION AND THE SEEK LOAD HEAD SWITCH MUST BE IN NEUTRAL POSITION WHEN EXECUTING IMPL IN CE MODE

OPERATE RESET SWITCH THEN IMPL SWITCH

PRESSURE PAD ACTUATOR LOAD

YES

NO

A5

B6

VOLTAGES OK

NO

YES

FIND YOUR SYMPTOM IN THIS CHART	PROBLEM	REPLACE CARDS	GO TO
ALL BYTES ARE THE SAME. NOTE: VERIFY YOUR DISPLAY PROCEDURE. PANEL 15, 16	SA-SB-SC-SD REGISTERS DID NOT RECEIVE DATA	B1P2 B2S2 B2D2 B2E2 B1N2	FSI 30
BYTE 0 COLUMN HAS COMMON CHARACTER AND SD HAS BYTE 2	GATING TO SA AND SC REGISTER FAILURE	B2D2	FSI 30
BYTE 1 COLUMN HAS COMMON CHARACTER AND SD HAS BYTE 3	GATING TO SB AND SD REGISTER FAILURE	B2E2	FSI 30
THE FIRST WORD IS CORRECT AND THE REST HAVE NO PATTERN	GATE FORCED IAR ADDRESS FAILURE. REFER TO MPL THEORY.	B2T2 B2S2 B2N2	FSI 30
WORDS '0000'-'000C' ARE CORRECT, '0444' AND/OR '3CCC' ARE INCORRECT.	HARDWARE IMPL WAS ABLE TO LOAD STORAGE BUT MICROPROGRAM COULD NOT LOAD STORAGE. SEE CHECKOUT PROCEDURE ON PANEL 30.	B2P2	FSI 30
'0000' = 00 6C 90 10 '0004' = 2F 10 F6 00	OVERLAY OF HARDWARE LOADER HAS OCCURRED. IF MPL FILE CYCLED TO TRACK 16, SPECIAL OPERATION 8 FAILED.	B1U4	FSI 30
NO PATTERN MATCHES ABOVE SYMPTOMS	HARDWARE IMPL FAILED TO STORE DATA	IMPL CHECK OUT	A4
UNUSUAL INDICATIONS OR CYCLES	BASIC TIMING OR GATING	CONSOLE CHECK	PANEL 30

WORD '0000' '000C'

E6

A5

ACTUATOR ATTEMPTED SEEK TO TRACK 0

YES

NO

A6

D6

IAR NOW = '00A8'

YES

NO

A8

G6

REPLACE IMPL DISK WITH SPARE. OPERATE RESET. OPERATE IMPL.

STILL FAILS

NO

YES

H6

INSTALL REMOVED IMPL DISK. SCOPE MPL FILE DATA: A-B1T4B09

DATA APPEAR OK

NO

YES

REPLACE

CU CARDS B1S2, B1T4, B2S2, B2N2

IF PROBLEM PERSISTS, PERFORM CE PANEL CHECKOUT

PANEL 30

A6

NO DATA FROM FILE OR DESERIALIZER FAILURE

B6

REPLACE

CU CARDS B1T4 B2S2. REFER TO ALD LA102 +3 ENGAGE MPL HEAD

TEST AND RETURN SCU TO CUSTOMER

D6

ADDRESS '00A8' IS MICROPROGRAM DETECTED READ OR SEEK CHECK ON THE MPL FILE

E6

IAR = '00A8'

YES

NO

A4

G6

OPERATE THE SEEK.LOAD HEAD SWITCH

SEEK IN-OUT OK

NO

YES

MPL 45

H6

MPL 15

D

A8

ST REGISTER BIT 3 ON

YES (READ CHECKS)

NO (SEEK CHECK)

PLACE CU IN CHECK STOP. OPERATE SEEK LOAD HEAD SWITCH (SEEK IN SEVERAL TRACKS AWAY FROM 0).

THE ADDRESS COMPARE SWITCHED MUST BE IN SYNC POSITION.

SEEK LOAD HEAD SWITCH MUST BE IN NEUTRAL POSITION WHEN EXECUTING IMPL IN CE MODE.

OPERATE RESET. OPERATE IMPL.

ACTUATOR PAD LOADS. ACCESS GOES TO TRACK 0. UNLOADS IMMEDIATELY.

NO

MPL 15

YES

SCOPE

A-B1T4J06 AND G09. OBSERVE FOR CIONCIDENT MINUS LEVELS WHILE EXECUTING IMPL

LEVELS OK

NO

MICROPROGRAM CONTROLLED SEEK PROBLEM

YES

REPLACE

CU CARDS B1T4 AND B1S2

MPL45

REPLACE

CU CARDS B2F2, B2S2, B1S2

TEST AND RETURN SCU TO CUSTOMER

PLACE CU IN CHECK STOP MODE. OPERATE THE SEEK/LOAD-HEAD SWITCH SEVERAL TIMES.

SEEK IN - OUT OK

NO

MPL 45

YES

REPLACE

CU CARDS B2F2, BIT4, B2S2.

MPL 50

MLM0002 437414
START 97-R
FA7 RCF875
LET. 8/6/73

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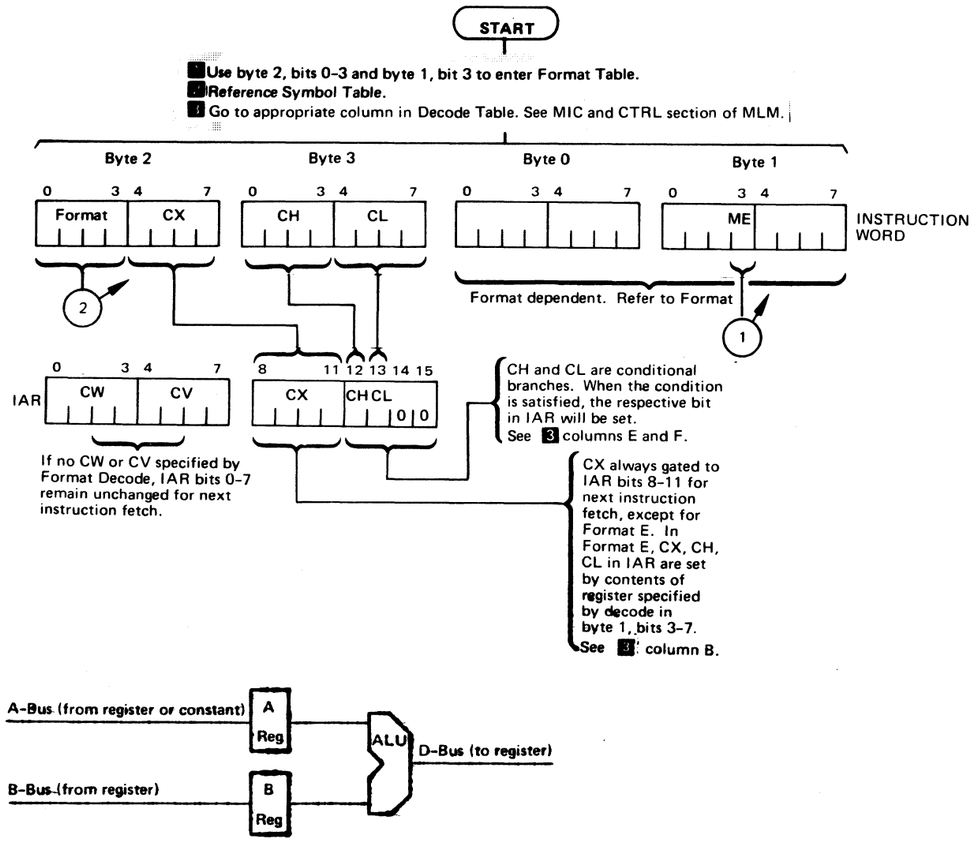
CU CLOCK STOPPED ANALYSIS (PART 3 OF 3) START 97

MICROINSTRUCTION FORMAT DECODE (Part 1 of 2)

- This page is used to decode an instruction read from control storage when no CAS printout is available.
- One word (four bytes) make up an instruction word.
- The four bytes are subdivided into control fields (see layout below).
- Byte 2, bits 4-7, and byte 3 are used for addressing of next word.
- Byte 2, bits 0-3, control the format to change the meaning of fields in bytes 0 and 1, ■ (Format Table).
- ■ (Symbol Table) explains the symbols used in ■
- ■ (Decode Table) on START 102 shows the operation controlled by each value in the fields in ■ .
- Details of formats are given in MIC section.
- Circuits of control unit are given in CTRL section.



Also used for Format Decode (1) (2)

■ 1

Format Table						Byte 0, 1 Decode													
Format	Byte 1		Byte 2			Byte 0								Byte 1					
	Bit 3	Bit 0	Bit 1	Bit 2	Bit 3	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
A	Ignore	1	0	0	0	CA				CV				ALU Op				CB/CD			
A	Ignore	1	0	0	1	CA				CV				ALU Op				CD			
A	Ignore	1	0	1	0	CA				CV				ALU Op				CB			
B	Ignore	1	0	1	1	CD***				CV				ALU Op				CB			
A	Ignore	1	1	0	0	CK								ALU Op				CB/CD			
A	Ignore	1	1	0	1	CK								ALU Op				CD			
A	Ignore	1	1	1	0	CK								ALU Op				CB			
C	Ignore	1	1	1	1	CW				CV				No ALU				CB			
D	0	0	0	0	0	CA				CS				ALU Op				CB/CD			
D	0	0	0	0	1	CA				CS				ALU Op				CD			
D	0	0	0	1	0	CA				CS				ALU Op				CB			
E	0	0	0	1	1	CA				CS				ALU Op				CB/CD			
D	0	0	1	0	0	CK*				CS				ALU Op				CB/CD			
D	0	0	1	0	1	CK*				CS				ALU Op				CD			
D	0	0	1	1	0	CK*				CS				ALU Op				CD			
F	0	0	1	1	1	XX		Sp Op		CS				No ALU	0	Spec Op					
1c	1	0	0	0	0	CK**				CS				ML				CB/CD			
3	1	0	0	1	0	NH				CS				ML	1	NL					
1a	1	0	1	0	0	CK**				CS				ML				CB/CD			
1b	1	0	1	0	1	CK**				CS				ML				CB/CD			
2a	1	0	1	1	0	MH				CS				ML				CB			
2b	1	0	1	1	1	MH				CS				ML				CB			

For additional format details, use format type and refer to MIC section of MLM.

Refer to symbol table for explanation and then go to ■ .

■ 2

Symbol Table	
CA	Hex value equals decode of register to be gated to A-bus input to ALU. See ■ column A.
CB	Hex value equals decode of register to be gated to B-bus input to ALU. See ■ Column B.
CD	Hex value equals decode of register to be gated from D-bus output from ALU. See ■ column B.
CB/CD	Indicates CB and CD above are same register.
CK	Hex value is a constant to be placed on the A-bus input to ALU.
CS	Hex value decodes to a set or reset of a specific ST register bit. Decode of DNST21 means if D-bus is nonzero for the current ALU Op, set ST register bit 2 to 1. See ■ column C.
CW	Hex value gated to IAR bits 0-3 for next instruction fetch.
CV	Hex value gated to IAR bits 5-7 or 4-7, (depending on format) for fetching of next instruction.
Spec Op	Hex value (byte 0, bits 2, 3 and byte 1, bits 4-7) activate hardware to perform unique functions. See MIC 5.
MH ML NH NL	Hex value gated to DAR for data fetch or store. See MIC section of MLM for specifics.
ALU Op	Hex value is decode of arithmetic operation to be performed. See ■ column D.

START 102

** If byte 2, bit 7 = 1, gate CK to A-register bits 0–3; bit 7 = 0, gate CK to A-register bits 4–7.*
*** Contents are gated to A-register bits 4–7.*
**** No A-bus input to ALU for this format.*

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MICROINSTRUCTION FORMAT DECODE (Part 1 of 2) START 100

MICROINSTRUCTION FORMAT DECODE (Part 2 of 2)

3

Symbol Value		Decode Table					
		A	B	C	D	E	F
Hex	Binary	CA	CB/CD	CS	ALU Op	CH ◆◆◆	CL ◆◆◆
00	00000	0◆	SA	———	A Ω B → D	0	0
01	00001	GC	SB	1 → ST 1	A • B → D	1	1
02	00010	ND	SC	DNST21	A ∀ B → D	Carry	D = 0
03	00011	NC	SD	1 → ST 3C	A + B → D	ST 0	Index ·ST 1
04	00100	TD	GB	1 → ST 0	A + B + C → DC	ST 2	ST 3C
05	00101	TC	GA	1 → ST 5	A - B + C → DC	ST 4	ST 5
06	00110	MD	TB	1 → ST 6	A + B → DC	ST 6	ST 7
07	00111	MC	NA	1 → ST 7	A – B + 1· → D	BR 0	BR 1
08	01000	GB	MB	0 → ST 4		BR 2★	BR 3★★
09	01001	GA	TA	0 → ST 1		BR 4★★★	BR 5★★★★
0A	01010	NB	TD	0 → ST 2		BR 6	BR 7
0B	01011	NA	MA	0 → ST 3C		CHK-2	SELTD/MC7
0C	01100	TB	MD	0 → ST 0		COMMO	HLTIO/XFER
0D	01101	TA	GC	0 → ST 5		ADDRO/MC6	SERVO/MULTI
0E	01110	MB	BR	0 → ST 6		SUPPO/XCHAN	CUEND/BFRDY
0F	01111	MA	MC	0 → ST 7		ILACT/BOPAR	RSPON/CHANB
10	10000		0◆◆				
11	10001		ST				
12	10010		GD				
13	10011		TG				
14	10100		ND				
15	10101		NC				
16	10110		NB				
17	10111		TC				
18	11000		GF	*See INTR 005 for feature cards.*			
19	11001		GE				
1A	11010		NF				
1B	11011		NE				
1C	11100		TF				
1D	11101		TE				
1E	11110		MF				
1F	11111		ME				

START 100

◆ *No register selected, A-bus input forced to '00'.*

◆◆ *Force B-bus to '00' (unless ALU Op 5 or 7, then force 'FF'). Force D-bus to '00'.*

◆◆◆ *See MIC 3 for further details.*

★ *During IMPL, BR 2 replaced by SECTR.*

★★ *During IMPL, BR 3 replaced by BTRDY.*

★★★ *During Inline, BR 4 replaced by INLIN.*

★★★★ *During Inline, BR 5 replaced by ILXEQ.*

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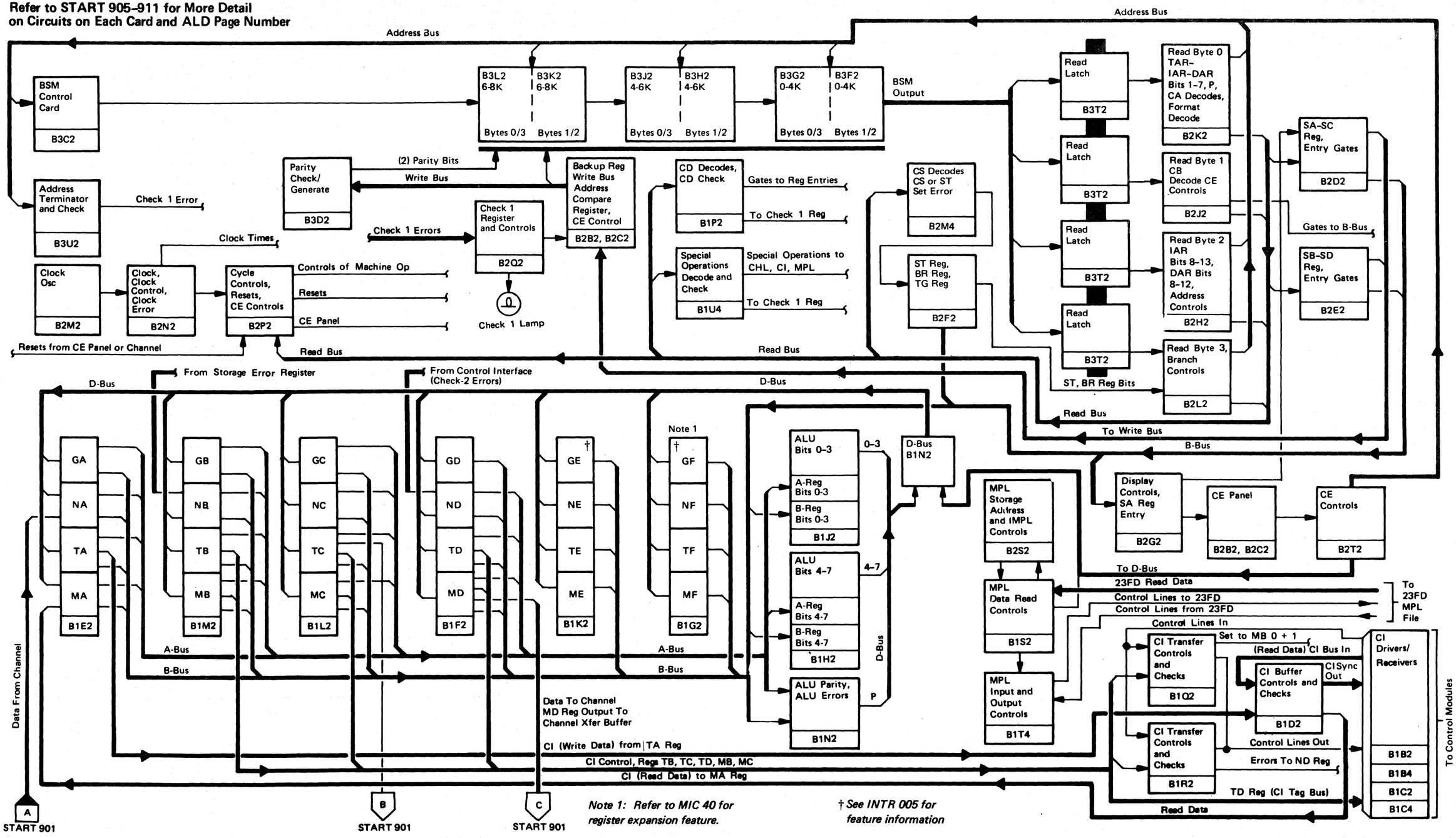
MICROINSTRUCTION FORMAT DECODE (Part 2 of 2) START 102

DATA FLOW BY CARD (Part 1 of 2)

Refer to START 905–911 for More Detail on Circuits on Each Card and ALD Page Number



Note 1: Refer to MIC 40 for register expansion feature.

† See INTR 005 for feature information

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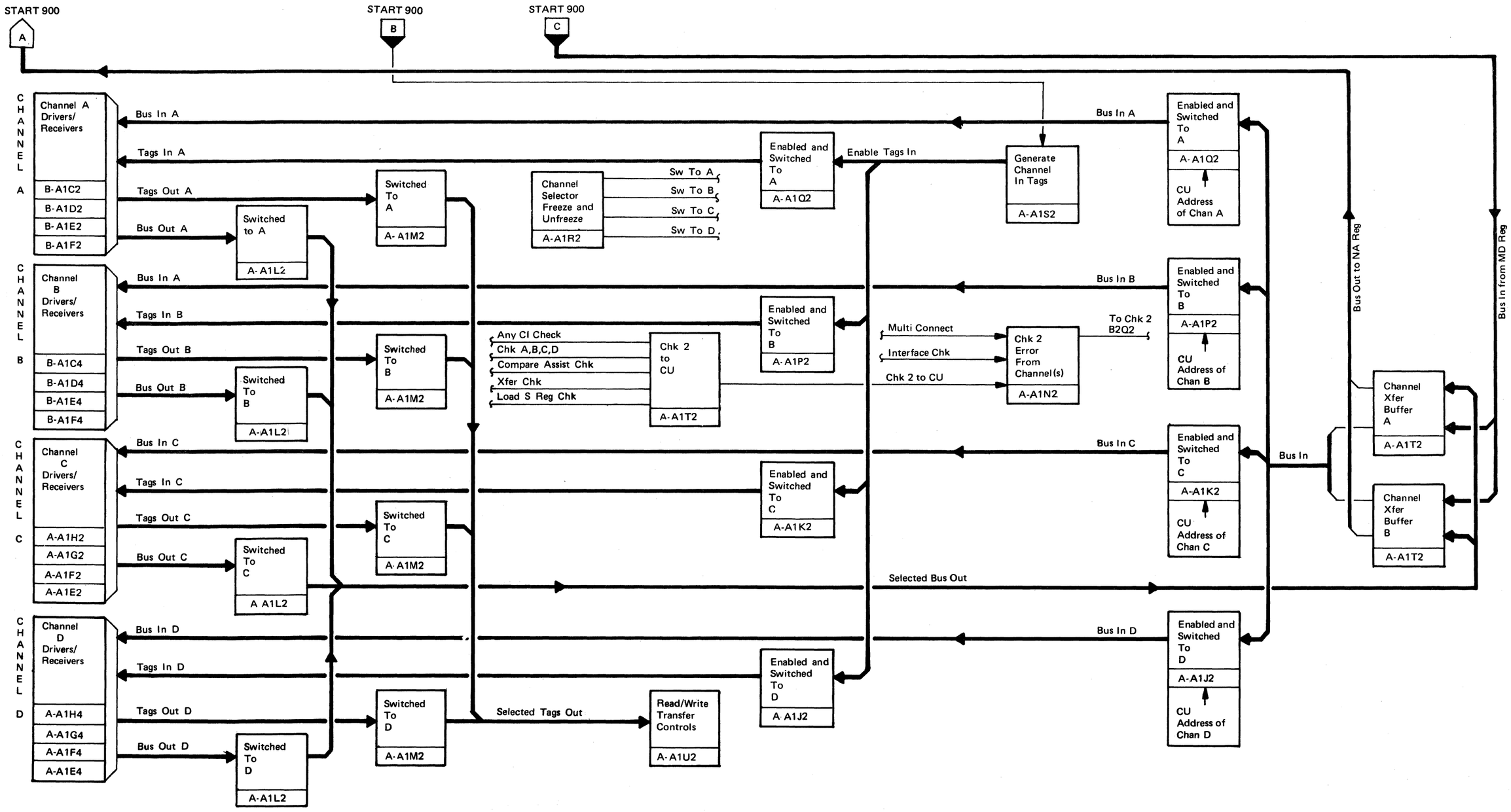
DATA FLOW BY CARD (Part 2 of 2)

Refer to START 905-911 for More Detail on Circuits on Each Card and ALD Page Number



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LIST OF CIRCUITS BY CARD (Part 1 of 7)

- This page lists the 3830–2 circuits by MST card to aid you in understanding what is happening when you swap cards.
- Cards with the same part number can be identified by the same reverse–printed letter: A B etc.
- For A–gate MST card part numbers, see microfiche card supplied with MLM.
- Error checking circuits are indicated by an asterisk (*).
- Refer to START 900 for card–level data flow.

A–A1D2 A *(Note 1)*

CHANNEL C SELECTION

Channel C Selection Relays CR101
Select Out/In C
Interface C Enabled
Allow Selection C CR102

A–A1D4 A *(Note 1)*

CHANNEL D SELECTION

Channel D Selection Relays DR101
Select Out/In D
Interface D Enabled
Allow Selection D DR102

A–A1E2 B *(Note 1)*

CHANNEL C RECEIVERS/DRIVERS

Channel C Bus Out Bits 4–7, P CA401
Channel C Bus In Bits 5–7 ..... CA402
Channel C Mark In

A–A1E4 B *(Note 1)*

CHANNEL D RECEIVERS/DRIVERS

Channel D Bus Out Bits 4–7, P DA401
Channel D Bus In Bits 5–7 ..... DA402
Channel D Mark In

A–A1F2 B *(Note 1)*

CHANNEL C RECEIVERS/DRIVERS

Channel C Out Tags CA301
Channel C Bus Out Bits 0–3
Channel C Bus In Bits 0–4, P CA302

A–A1F4 B *(Note 1)*

CHANNEL D RECEIVERS/DRIVERS

Channel D Out Tags DA301
Channel D Bus Out Bits 0–3
Channel D Bus In Bits 0–4, P DA302

A–A1G2 B *(Note 1)*

CHANNEL C RECEIVERS/DRIVERS

Channel C Out Tags CA201
Channel C In Tags CA202

A–A1G4 B *(Note 1)*

CHANNEL D RECEIVERS/DRIVERS

Channel D Out Tags DA201
Channel D In Tags DA202

A–A1H2 B *(Note 1)*

CHANNEL C RECEIVERS/DRIVERS

Channel C Out Tags CA101
Channel C In Tags CA102

A–A1H4 B *(Note 1)*

CHANNEL D RECEIVERS/DRIVERS

Channel D Out Tags DA101
Channel D In Tags DA102

A–A1J2 C *(Note 1)*

CHANNEL D CONTROLS

Trap Select Out D KD101
Select Out Latched D
System Reset Chan D
Selective Reset D
Request In D
Selected and Sw to D
Propagate Select Out D
Cmmd Out/Halt to D KD102
CU Busy D
CU End D
Halt I/O or Busy D
Operational in D
Address In D
Status In D
Address Compare D KD103
Channel D Bus Out Parity Error
Select Out Delayed D KD104
CU Address Bits 0–4 (Jumpers) Ch D
Enabled D KD105
Metering In D
Run Meter D
*Interface Check Chan D KD106
System Reset Latched D
Machine Reset D

A–A1K2 C *(Note 1)*

CHANNEL C CONTROLS

Trap Select Out C KC101
Select Out Latched C
System Reset Chan C
Selective Reset C
Request In C
Selected and Sw to C
Propagate Select Out C
Cmmd Out/Halt to C KC102
CU Busy C
CU End C
Halt I/O or Busy C
Operational In C
Address In C
Status In C
Address Compare C KC103
Channel C Bus Out Parity Error
Select Out Delayed C KC104
CU Address Bits 0–4 (Jumpers) Ch C
Enabled C KC105
Metering In C
Run Meter C
*Interface Check Chan C KC106
System Reset Latched C
Machine Reset C

A–A1L2 D

SELECTED CHANNEL DATA AND CONTROLS

Seltd Bus Out Bits 0–4 ..... NE201
Seltd Bus Out Bits 5, 7, P NE202
Seltd System Reset
Seltd Command Out
Seltd Address Bits 0, 1 ..... NE203
*Multi Connect 2 ..... NE204

A–A1M2 D

SELECTED CHANNEL DATA AND CONTROLS

Address Out Seltd NE101
COMMO–Set CH12
Seltd Sw to (Set CL11)
Suppress Out
Seltd Data Out
Seltd Bus Out Bit 6 ..... NE102
Seltd Service Out
Seltd Selective Reset
HIO or Busy Seltd
Bus Out Parity Error Seltd
CUEND B/C/D NE103
Enable CUEND B/C/D
Seltd Addr Bit 2, 3, 4
*Multi Connect 1 ..... NE104

A–A1N2

SELECTED CHANNEL CONTROLS

Seltd Op In DL101
*Check 2 to CCU
*Chk A•Sw to A+Chk C•Sw to C
*Chk B•Sw to B+Chk D•Sw to D
Special Selective Reset DL102
Allow Disable Chan A

Note 1: Only with Two Channel Switch, Additional, feature.

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LIST OF CIRCUITS BY CARD (Part 2 of 7)

A–A1P2 C †

CHANNEL B CONTROLS

Trap Select Out B. KB101
Select Out Latched B
System Reset Chan B
Selective Reset B
Request In B
Selected and Sw to B
Propagate Select Out B
Cmmd Out/Halt to B KB102
CU Busy B
CU End B
Halt I/O or Busy B
Operational In B
Address In B
Status In B
Address Compare B. KB103
Channel B Bus Out Parity Error
Select Out Delayed B. KB104
CU Address Bits 0–4 (Jumpers) Ch B
Enabled B. KB105
Metering In B
Run Meter B
*Interface Check Chan B KB106
System Reset Latched B
Machine Reset B

A–A1Q2 C

CHANNEL A CONTROLS

Trap Select Out A KA101
Select Out Latched A
System Reset Chan A
Selective Reset A
Request In A
Select and Sw to A
Propagate Select Out A
Cmmd Out/Halt to A. KA102
CU Busy A
CU End A
Halt I/O or Busy A
Operational In A
Address In A
Status In A
Address Compare A. KA103
Channel A Bus Out Parity Error
Select Out Delayed A. KA104
CU Address Bits 0–4 (Jumpers) Ch A
Enabled A KA105
Metering In A
Run Meter A
*Interface Check Chan A KA106
System Reset Latched A
Machine Reset A

A–A1R2

CHANNEL SWITCHING

Switched to A, B, C, D (Tie Breaker) CS101
Freeze and Unfreeze CS102
Enable CU Busy A, B, C, D
Trap and Select A, B, C, D (Jumpers) CS103
Allow Disable Chan B, C, D
Set Bus Bits, 1, 3, P Ch B, C, D CS104
SUPPO/XCHAN–Set CH14

A–A1S2

ERROR 1 DISCONNECT CONTROLS

Disconnect In. GK701
Request In A, B Under Error
Prop Select Under Error
Enable Address In
Enable Op In
SERVO/MULTI–Set CL13
Selective Reset Gated (by Error) GK702
ILACT/BOPAR–Set CH15
*Xfer Check

A–A1T2

CHANNEL TRANSFER BUFFERS

Buffer A or B Bits 0, 1, 2 . . . . . GK601
External Bits 0, 1, 2 to NA Reg
Sel Address Bit 2 (Jumper)
Buffer A or B Bits 3, 4, 5 . . . . . GK602
External Bits 3, 4, 5 to NA Reg
Buffer A or B Bits 6, 7, P GK603
External Bits 6, 7 to NA Reg
External Bit P to NA Reg GK604
*Buffer Parity Check
*Check 2 to CCU
*Mprog•Ch Resp Miscompare
Ext Gating to NA Reg. GK605

A–A1U2

CHANNEL TRANSFER CONTROL

Chan Write Mode Latched. GK501
Chan Read Mode Latched
Freeze Latch GK501
Read or Write Enabled
Microprog Response Latch GK502
Channel Response Latch
Transfer Latch A, B GK503
Data In
Service In
Sample Read Parity Error
Set Buffer A, B. GK504
Steer Bfr A to NA or Bus In
*Transfer Counters Miscompare GK505
Shutdown of Channel Transfer
CUEND/BFRDY–Set CL14 . . . . . GK506
HLTIO/XFER–Set CL12

† *See INTR 005 for feature cards.*

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A–B1B2 H

CTL–I RECEIVERS/DRIVERS

CI Bus In Bits 6, 7, P GA701
CI Sync In
CI Select Active
CI Tag Valid
CI Bus Out Bits 0–5 ..... GA702

A–B1B4 H

CTL–I RECEIVERS/DRIVERS

CI Unselected Alert 1 ..... GA401
CI Bus Out Bits 6, 7, P GA402
CE Communication Out
CI Tag Bus Bit 3

A–B1C2 H

CTL–I RECEIVERS/DRIVERS

CI Bus In Bits 0–5 ..... GA601
CI Tag Bus Bits 0, 4–7, P GA602

A–B1C4 H

CTL–I RECEIVERS/DRIVERS

CI Normal End GA501
CI Check End
CI Selected Alert 1–3
CI Select Hold GA502
CI Tag Gate
CI Response
CI Sync Out
CI Recycle

A–B1D2

CTL–I BUFFER AND CONTROL

CI Buffer Bits 0–7, P GA101
*CI Buffer Parity Error
Generated Bit P to MA
CI Bus Out Bits 0–7, P GA102
*CI Bus Out Parity Check
Control Decodes GA103
Not Data Response
CI Write
CI Read–Load S Reg
Sync Out
Buffer Full Latch
CH 5 Branch Latch GA103
Sync In Latch
Sync In Detected GA104
Norm End or Chk End Deskewed
Gate CI Bus In to Buffer
Gate External Data to MA Reg
*CI Transfer Error
1st Sync In

A–B1E2 J

GP REGISTER GROUP A

TA Reg Bits 0–7, P. RG101
MA Reg Bits 0–7, P RG102
NA Reg Bits 0–7, P RG103
GA Reg Bits 0–7, P RG104
D Bus Bits 0–7, P to TA, MA, NA
A Bus 1 Bits 0–7, P RG105
*CA Decode 9, 11, 13, 15 Even
B Bus 1 Bits 0–7, P RG106
*CB Decode 5, 7, 9, 11 Even

A–B1F2 J

GP REGISTER GROUP D

TD Reg Bits 0–7, P. RG401
MD Reg Bits 0–7, P RG402
ND Reg Bits 0–7, P RG403
GD Reg Bits 0–7, P RG404
D Bus Bits 0–7, P to TD, MD, ND
A Bus 4 Bits 0–7, P RG405
*CA Decode 2, 4, 6 Even
B Bus 4 Bits 0–7, P RG406
*CB Decode 10, 12, 18, 20 Even

A-B1G2

GP REGISTER GROUP F

TF Reg Bits 0–7, P RG601
MF Reg Bits 0–7, P. RG602
NF Reg Bits 0–7, P. RG603
GF Reg Bits 0–7, P. RG604
D Bus Bits 0–7, P to TF, MF, NF
B Bus 5 Bits 0–7, P. RG605
*CB Decode 24, 26, 28, 30

A–B1H2 K

ALU AND INPUT REGS A AND B

A and B Reg Bits 6 and 7 ..... RA101
A and B Bus Asm Bits 6 and 7
A and B Reg Bits 4 and 5 ..... RA102
A and B Bus Asm Bits 4 and 5
ALU Sum Bits 6 and 7 ..... RA103
ALU Sum Bits 4 and 5 ..... RA104

A–B1J2 K

ALU AND INPUT REGS A AND B

A and B Reg Bits 2 and 3 ..... RA201
A and B Bus Asm Bits 2 and 3
*A Reg Parity Error
A and B Reg Bits 0 and 1 ..... RA202
A and B Bus Asm Bits 0 and 1
*B Reg Parity Error
ALU Sum Bits 2 and 3 ..... RA203
ALU Sum Bits 0 and 1 ..... RA204

A–B1K2 †

GP REGISTER GROUP E

TE Reg Bits 0–7, P RG501
ME Reg Bits 0–7, P RG502
NE Reg Bits 0–7, P. RG503
GE Reg Bits 0–7, P. RG504
D Bus Bits 0–7, P to TE, ME, NE
B Bus 5 Bits 0–7, P RG505
*CB Decode 25, 27, 29, 31 Even

A–B1L2 J

GP REGISTER GROUP C

TC Reg Bits 0–7, P. RG301
MC Reg Bits 0–7, P RG302
NC Reg Bits 0–7, P RG303
GC Reg Bits 0–7, P RG304
D Bus Bits 0–7, P to TC, MC, NC
A Bus 3 Bits 0–7, P RG305
*CA Decode 1, 3, 5, 7 Even
B Bus 3 Bits 0–7, P RG306
*CD Decode 13, 15, 21, 23 Even

A–B1M2 J

GP REGISTER GROUP B

TB Reg Bits 0–7, P. RG201
MB Reg Bits 0–7, P RG202
NB Reg Bits 0–7, P RG203
GB Reg Bits 0–7, P RG204
D Bus Bits 0–7, P to TB, MB, NB
A Bus 2 Bits 0–7, P RG205
*CA Decode 8, 10, 12, 14 Even
B Bus 2 Bits 0–7, P RG206
*CB Decode 4, 6, 8, 22 Even

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LIST OF CIRCUITS BY CARD (Part 4 of 7)

A–B1N2

ALU OPS, PARITY, D BUS

ALU Parity Predictor RA301
A and B Reg P Bits
Carry Out Latch
ALU Bit P for Non XOR Op
A Reg P and B Reg P Even
D Equal Zero Check RA302
Machine Reset Dlyd
*ALU Check RA303
Carry In to ALU
Store Carry Out
ALU Operation Decodes
CE Data Bits 0–7, P RA304
D Bus Bits 0–7, P RA305

A–B1P2

CD DECODE AND REGISTER SETS

Gate CD 16–31 ..... DE101
Block CD Decode
Gate Read Byte 1 to CD
Gate Read Byte 0 to CD
Clock Pulses to CD
CD Decodes DE102
*CD Field Parity Check
Sets to SA, SB, SC, SD DE103
Gate ST Reg
Sets to MA, MB, MC, MD, ME
NA, NB, NC, ND, NE Reg DE104
Sets to TA, GA, TB, GB, TD, GC,
TC, BR, TE, GD, GE, TG Reg DE105
Odd Sets to GP Out of 25 ..... DE106
Odd Sets to GP Out of 5
*CD Decode Error DE107

A–B1Q2

CTL–I CONTROLS

CI Recycle Latch GA201
*Unexpected End Chk
ADDRO/MC6–Set CH13
SELTD/MC7–Set CL11
CB Decode 0–3
S Reg Decode (MA to SA–SD) GA202
*Load S Reg Check
ST 4 CH 5 Branch
Tag Valid Synced
Gate MB Reg GA203
Set D Bus Not Zero to MB Bit 1
Set Carry to MB Bit 0 ..... GA203
Set MB Bit P
*Compare Assist Check
Index Latch

A–B1R2

CTL–I CONTROLS

*Tag Bus Parity Check GA301
*Select Active Check
*Controller Check
Set Buffer
RSPON/CHANB–Set CL15
Response Latch GA302
*Any CI Check
Bit P to ND
Buffer Parity Chk or Sync In–ND2
Norm End or Tag Bus Parity Chk–ND4
Chk End or Bus Out Parity Chk–ND5
Tag Valid or Xfer Chk–ND6

A–B1S2

MPL FILE DESERIALIZER

Data Separator Count Control LA301
80 and 160 nsec FF
B Time Pulse (Drive & B2)
Data Separator Count LA302
10•24, 20•48 usec FFs
320, 640 nsec FFs
Data Strobe
B Time Pulses (B2, B3, B4)
Data Separator and Data Input LA303
Gate Incr Data Sep Count
Data Detector
Data Bit
MPL File Read Latch
Reset Storage Error Reg
Storage Diagnostic Mode
Bit Counter and Control LA304
Wait Latch
Set Byte Assembler Bits 0–7, P
Parity Time
MPL Data Byte Bits 0–7, P LA305
Byte Assembler and Count Control LA306
Byte Ready CL8
Error or Sector CH8
*MPL File Rd Chk to Chk–1 Reg
IMPL Error
Retry Sector Read (Sector Non Zero)
MPL Data Byte Bit P Correct
Track is Not Zero

A–B1T4

IMPL CONTROL

MPL Input Control Lines LA101
MPL Output Control Lines LA102
TG Reg Bits 0–2 (to Chan Interface)

A–B1U4

SPECIAL OPERATIONS DECODE

Partial Decode DE401
Special Operations 0–12, 14, 16,
18, 20, 22 ..... DE402
*Special Operation Error DE403
Special Operations 13, 15, 17, 19,
21, 23, 24, 26, 28, 30 ..... DE404
*Spec Op 24–31 Even

A–B2B2 L

BAR, ACR, DISPLAY CONTROL (HIGH BYTES)

ACR–Prog Display Decode RL301
Addr Display Decode
Chk 1 Display Decode
BAR Display Decode
Write Gate SA, SC
Write Gate Chk 1
Backup Addr Reg Bits 0–7, P RL302
Address Bus Bits 0–7, P
Write Bus Byte 0, Bits 0–7, P RL303
Addr Compare Reg Bits 0–7, P RL304
CE Addr Hi Byte Bits 0–7
Addr–Chk–Prog Disp Bits 0–7, P RL305
Write Bus Byte 2 Bits 0–7, P RL306
Compare Equal (ACR and Address Bits) RL307

A–B2C2 L

BAR, ACR, DISPLAY CONTROL (LOW BYTES)

ACR–Prog Display Decode RL401
Addr Display Decode
Chk 1 Display Decode
BAR Display Decode
Write Gate SB, SD
Write Gate Chk 1
Backup Addr Reg Bits 0–7, P RL402
Address Bus Bits 0–7, P
Write Bus Byte 1 Bits 0–7 ..... RL403
Addr Compare Reg Bits 8–15, P RL404
CE Addr Lo Byte Bits 0–7
Addr–Chk–Prog Disp Bits 8–15, P RL405
Write Bus Byte 3 Bits 0–7, P RL406
Compare Equal (ACR and Address Bits) RL407

A–B2D2 M

STORAGE REGISTERS SA, SC

Storage Reg SA Bits 0–3 ..... RS101
Gate D Bus to SA Reg
*CB Decode 0,2 Even
Gate External Byte 0 to SA
Gate SA Asm Byte to SA
Storage Reg SA Bits 4–7, P RS102
Storage Reg SC Bits 0–7, P RS103
Gate D Bus to SC Reg
Gate External Byte 2 to SC
Gate Read Byte 2 to SC

A–B2E2 M

STORAGE REGISTERS SB, SD

Storage Reg SD Bits 0–3 ..... RS201
Gate D Bus to SD Reg
Gate Read Byte 3 to SD
Gate External Byte 3 to SD
*CB Decode 1, 3 Even
Storage Reg SD Bits 4–7, P RS202
Storage Reg SB Bits 0–7, P RS203
Gate D Bus to SB Reg
Gate Read Byte 1 to SB
Gate External Byte 1 to SB

A–B2F2

ST, BR, TG REGISTERS

Stat Reg Bits 0–7 ..... RB101
Stat Reg Bit P RB102
Branch Register Bits 0–7, P RB103
D–Bus Bits 0–7, P to ST, TG, BR
TG Reg Bits 0–7, P RB104
TG Reg Bits 0–3 Special Out
TG Reg Bit 4 Block Sw to D
TG Reg Bit 5 Block Sw to C
TG Reg Bit 6 Block Sw to B
TG Reg Bit 7 Block Sw to A
B–Bus 7 Bits 0–7, P RB105
*CB Decode 1, 3, 17, 19 Even
B–Bus 8 Bits 0–7, P RB106
*CB Decode 0, 2, 14 Even

A–B2G2

SA AND DISPLAY ASSEMBLERS

Gate Byte 0/1/2/3 to SA Reg RS301
Reg Sel or Ext Disp Sw Pos
Gate B Bus Assem to Display
Gate User Data to Display
Assembled Rd Bus Bits 0–2 to SA RS302
Bits 0–2 to Reg–Stor Display
Assembled Rd Bus Bits 3–5 to SA RS303
Bits 3–5 to Reg–Stor Display
Assembled Rd Bus Bits 6, 7, P to SA RS304
Bits 6, 7, P to Reg–Stor Display

A–B2H2

IAR, DAR, FORMAT DECODE, ADDRESS BUS

Read Byte 2 Bits 0–7, P RL101
Set IAR Bit P 8–13
IAR Bits 8–13, P RL102
DAR Bits 8–12 ..... RL103
Storage Address Bus Bits 8–12
Gate DAR to Address Bus
Inhibit IAR to Address Bus
Gate B Bus to Address Bus
Gate IAR to Address Bus
DAR Bits 13–15, P RL104
Storage Address Bus Bits 13–15, P
*Storage Addr Bus 8–15 Error
Gate NH–NL to DAR Low
Gate B Assembler to DAR Low
Format Decodes RL105
Gate A Bus to A–Reg
CA Decode 11 NA to User
Gate CK 4–7 to A–Reg 4–7
ME Bit Equal 1
Spec Op Valid
Gate CK 0–3 to A–Reg 4–7
Gate CK 0–3 to A–Reg 0–3
0–3 P Bit to A–Reg
Block CD Decode
Gate Read Byte 0 to CD
Gate Forced Addr to IAR Low
Gate B Bus to B Reg
Gate CX to IAR Low
Gate B Assembler to IAR Low

A–B2J2

CB DECODE, ADDR COMPARE CONTROL

CB Partial Decode DE501
Store Rd Bus Byte 1 Bits 0–7, P
CB Decodes 0–23 ..... DE502
CB Decodes 24–31 ..... DE503
*CB Even Decode Error DE504
*CB Odd Decode Error
Read Bus Byte 1 Parity 3–7
Read Bus Byte 1 Parity 4–7
Read Bus Byte 1 Parity 0–2
CE Reg Sel Sw Bits 1, 2, 4, 8, 16
Addr Comp Ind Sw DE505
Addr Comp Force Clk Stp 2
Addr Comp Sync 2

A–B2K2

IAR, DAR, TAR, CA DECODE, FORMAT DECODE

Stor Rd Bus Byte 0 Bits 0–7, P RL201
CA Decodes 0–15 ..... RL202
TAR Bits 1–4 ..... RL203
IAR Bits 1–4
Set TAR or Force Addr
TAR Bits 5–7, P RL204
IAR Bits 5–7, P
DAR Bits 1, 2, P RL205
Stor Addr Bus Bits 1, 2, P
DAR Bits 3–7 ..... RL206
Stor Addr Bus Bits 3–7
Instr Format Decodes RL207
Gate TAR to IAR
Gate CW 1–3 to IAR
Gate CV 4–7 to IAR
FM and KK
FM and KK Not
ND and NB
Gate 0 to DAR
Gate MH 1–4 to DAR
TAR 0–3 Parity Bit RL208
TAR 0–4 Parity Bit
*CA Even Decode Error
Read Byte 0 Parity 4–7
Read Byte 0 Parity 5–7
*CA Odd Decode Error
Read Byte 0 Parity 0–4
Read Byte 0 Parity 0–3
Set DAR Bit P 0–7
Set IAR Bit P 0–7 ..... RL211
*Address Bus 0–7 Parity Error

A–B2L2

CH, CL DECODE

Read Byte 3 Bits 0–7, P
BR 2–5 Branch Conditions
CH Branch Bit DE302
CH Branch Bit Compare DE303
CL Branch Bit DE304
Index–ST1 Br Condition
CL Branch Bit Compare DE305
*Branch Error DE306
Spec Op 7 Latched
Ext CH Branch Cond 12–15
Ext CL Branch Cond 11–15
Gate CL 3
ST Register Bits 0–7, P Ext DE307
*ST Reg Parity Error

A–B2M2

CU CLOCK DRIVE

25 MHz Oscillator KK101
X Drive
Y Drive
Clocked System Reset KK102
Execute Sw 85–ns Pulse KK103

A–B2M4

CS DECODE

CS Decode DE201
Set Reset ST 0–3
Gate Err 1 Reg to Wr Bus
*CS Field or Stat Set Err
Inst Cycle and Not FM
Set Reset ST 4–7 ..... DE202
*Stat Set Error
Reset or CD Equal Stat
Gated Store Carry

A–B2N2

CU CLOCK AND OUTPUTS

CU Clock Stopped Latch KK201
*CU Clock Error
Block BAR Set
CU Clock Ring KK202
CE Pnl Enter to Storage KK203
Store Cycle
Write into Storage
Execute Sw or IMPL Set Pulse KK203
IMPL Ld IAR and S Reg
CE Pnl Fetch to Storage
BC Blocked by Data Cycle
Set A, B Regs KK204
Set to CD Field
Go to Storage
Set IAR, A, B, C
40 ns Pulse
Clock Pulses Powered KK205
Set Storage Read Latches
Set BAR Not Call
Set D0 and Carry Ltch CDEF CL
Reset IAR Ctrl Ltch
Stat 3 CL and Op Decode
Stat 2 CH and CS Decode

A–B2P2

CU CYCLE CONTROL, RESETS, ADDRESS COMPARE

Not Access Cycle KK301
Instruction Cycle
Instruction Call Cycle
Data Cycle
*CU Cycle Error
Store Early Decision KK302
Store Call Cycle
Data Fetch Cycle
Data Fetch 4–Byte Cycle
Sys or Sel Rst Start CU Clk KK303
Reset Request Stop CU Clock
Sel Rst Gated by CU Clock
Machine Reset
Machine Reset to Chk 1 Reg
Reset to TA, TB, TD Reg
Addr Compare Force Recycle KK304
Addr Comp Force Clock Stop
Addr Compare Latched
Addr Compare Sync ACR

LIST OF CIRCUITS BY CARD (Part 6 of 7)

A–B2Q2

CHECK 1 REGISTER AND CONTROLS

Block Wr Bus 1, 3 Error RC101
Block Error Bits 4 and 5
Block ECC or Wr Bus 0, 2 Error
Block ALU Error
Store Call Cycle Latched
Block Stor Mult Error
Set Error Detectors
Set Check 1 Reg A, B, C
Check 1 Register Bits 2–7 . . . . . RC102
Check 1 Entry Latches Bits 2–7
Check 1 Reg Bits 8–13. . . . . RC103
Check 1 Entry Latches Bits 8–13
Check 1 Reg Bits 0, 1. . . . . RC104
Check 1 Reg Bit P 0–7, 8–15
Check 1 Entry Latches Bits 0, 1
Early Error
Check 1 Error
CE Check Stop Mode
CE Check Bypass Mode
Not Check 1 Latch RC105
Interface Disc Latch (Check 1 to User)
Error Stop to Clock
Check 2 Latch
Check 2 Branch
Error or Sys Reset 1, 2, 3
Gate Chk 1 Reg to Wr Bus
Block Set BAR
Check 2 Reset or Machine Reset
CD Decode Error Latched
Reset to TC, TE, TF, TG, ST Reg
Set Storage Error Reg

A–B2S2

IMPL CONTROL

Byte Counter Bits 8–15 . . . . . LA201
IMPL Addr Bits 8–13, P to IAR
Set IAR and Set S Reg
IMPL Start Clock
Store Pulse
Gate Ext Data to SA, SB, SC, SD LA202
CE Gate Read Byte 1 to CD
IMPL Ext Data to SD
Gate MPL Data to D Bus
Gate IAR to Stor
Sector Error Counter LA203
Auto Read Latch LA204
MPL File Engage Head Hdware
Halt IMPL or Not IMPL Latch
MPL Not Rdy to Chk 1 Reg LA204
MPL File Force Access Out
CE Bypass or Chk Stop Mode
IMPL Latch. LA205
MPL On
End IMPL Latch

A–B2T2

CE ADDRESS GATING AND INLINE CONTROLS

Start Switch Latch KP101
Reset Switch Latch
SI–Stop Switch Latch
Normal or Inline Mode
Check Reset Latch
CE Mode Check Reset
Execute Switch Latch
CE Mode Execute Switch
Forced Address Bit 1–7, P Hi. KP102
Forced Address Bit 8–13, P Lo KP103
Enter/Display ACR KP104
Display Control 1 and 2
Prog Data Entry–Display
Normal Mode
Inline Mode
IMPL Gate
Any Interrupt
Gate Forced Address to IAR
Gate CE Address to IAR
Machine Reset to 0000
Selective Reset to 0040
Inline CH 9 Branch KP105
Inline CL 9 Branch
Gate CE Data to D Bus
Set ACR

A–B3C2

BSM Control SW50x
Read Data Bits C4, C5 . . . . . SW439

A–B3D2

WRITE BUS PARITY CHECK/GENERATE

Read Data Bits C0, C1 . . . . . SW441
Bytes 0 and 2 . . . . . SW521
Bytes 1 and 3 . . . . . SW522

A–B3F2

4Kx34 STORAGE ARRAY

0-4K, Bytes 1 and 2. . . . . SW562
4K Address Decode SW562

A–B3G2

4Kx34 STORAGE ARRAY

0-4K, Bytes 0 and 3. . . . . SW561
4K Address Decode SW561

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LIST OF CIRCUITS BY CARD (Part 7 of 7)

A–B3H2

2Kx34 STORAGE ARRAY

4 to 6K, Bytes 1 and 2 . . . . . SW564
2K Address Decode SW564

A–B3J2

2Kx34 STORAGE ARRAY

4 to 6K, Bytes 0 and 3 . . . . . SW563
2K Address Decode SW563

A–B3K2

2Kx34 STORAGE ARRAY

6 to 8K, Bytes 1 and 2 . . . . . SW566
2K Address Decode SW566

A–B3L2

2Kx34 STORAGE ARRAY

6 to 8K, Bytes 0 and 3 . . . . . SW565
2K Address Decode SW565

A–B3T2

READ LATCHES

Byte 0 . . . . . SW511
Byte 1 . . . . . SW512
Byte 2 . . . . . SW513
Byte 3 . . . . . SW514

A–B3U2

ADDRESS CHECK AND TERMINATORS

Address Check SW553
Block Go SW553
Address Bit 2 . . . . . SW552
Terminators SW558

B–A1C2 B

CHANNEL A RECEIVERS/DRIVERS

Channel A Out Tags AA101
Channel A In Tags AA102

B–A1C4 B †

CHANNEL B RECEIVERS/DRIVERS

Channel B Out Tags BA101
Channel B In Tags BA102

B–A1D2 B

CHANNEL A RECEIVERS/DRIVERS

Channel A Out Tags AA201
Channel A In Tags AA202

B–A1D4 B †

CHANNEL B RECEIVERS/DRIVERS

Channel B Out Tags BA201
Channel B In Tags BA202

B–A1E2 B

CHANNEL A RECEIVERS/DRIVERS

Channel A Out Tags AA301
Channel A Bus Out Bits 0–3
Channel A Bus In Bits 0–4, P AA302

B–A1E4 B †

CHANNEL B RECEIVERS/DRIVERS

Channel B Out Tags BA301
Channel B Bus Out Bits 0–3
Channel B Bus In Bits 0–4, P BA302

B–A1E6 A

CHANNEL A SELECTION

Channel A Selection Relays AR101
Select Out/In A
Interface A Enabled
Allow Selection A. AR102

B–A1F2 B

CHANNEL A RECEIVERS/DRIVERS

Channel A Bus Out Bits 4–7, P AA401
Channel A Bus In Bits 5–7 . . . . . AA402
Channel A Mark In

B–A1F4 B †

CHANNEL B RECEIVERS/DRIVERS

Channel B Bus Out Bits 4–7, P BA401
Channel B Bus In Bits 5–7 . . . . . BA402
Channel B Mark In

B–A1F6 A †

CHANNEL B SELECTION

Channel B Selection Relays BR101
Select Out/In B
Interface B Enabled
Allow Selection B. BR102

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PREVENTIVE MAINTENANCE - 3830 STORAGE CONTROL, MODEL 2

PREVENTIVE MAINTENANCE - 3830 STORAGE CONTROL, MODEL 2 **START 950**

Code U	Code R	Location/Unit	Frequency	Lubricate/Clean Replace/Check	Observe	Reference/Procedure
1		Filters: Logic Gate and Power Supplies	3 Months	Check - Replace if Required	If gate or power supply filters are excessively dirty, increase frequency of filter inspection	**Logic Gate Filter** 1. Open rear CU cover 2. Remove old filter by pulling downward 3. Vacuum the filter area (if required) 4. Install new filter 5. Verify that gate fans are running **Power Supply Filters** 1. Open front CU cover 2. Loosen retaining straps and remove old filters (2) 3. Vacuum the filter area (if required) 4. Install new filters 5. Verify that power supply cooling fans are running
6		General Machine Check	6 Months	Check	Check primary ac cables for wear and safe condition. Check covers for appearance.	

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PREVENTIVE MAINTENANCE - 3830 STORAGE CONTROL, MODEL 2 START 950

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PERFORMANCE DATA COLLECTION

STATISTICAL DATA COLLECTION

Format

The Operating System (OS) collects 24 bytes of format 6 sense data. (See SENSE 25.) OS adds time, date, device type, channel/unit address, physical drive/CU ID, and volume ID (pack label). OS formats the data and writes it to SYS1.LOGREC as an I/O statistical record.

Method of Collection

1. When OS issues a pack dismount message to the operator, it executes a Read and Reset Buffered Log sense command (CMD 145) and records statistics. This permits gathering statistical information that is related to each disk pack as well as to each drive.
2. When the operator issues a Halt EOD (End of Day) command in order to terminate OS, the operating system issues Read and Reset Buffered Log and records statistics as part of its shutdown procedure. When shutdown is completed, it replies EOD successful. The operator then powers down the system.
3. When a drive error or usage counter (in control storage) exceeds its predetermined threshold (error counter), or overflows (usage counter), the data is collected.

USAGE/ERROR THRESHOLD VALUES	
Bytes read	$2^{31}-1$
Access motions	$2^{15}-1$
Correctable data checks	512
Retry data checks	64
Seek errors	8

To collect the data, a Read And Reset Buffered Log is initiated by the CU as follows:

a. The next Start I/O addressing that drive is not executed. Instead, initial status presents Unit Check status to OS.
b. As a result of receiving Unit Check status, OS issues a Sense command which transfers the sense data to the system for analysis. The Sense command resets the sense data following the transfer.

Note: If this was caused by an error counter exceeding its threshold, the drive enters logging mode at this time.

c. System error recovery procedures (ERPs) determine that the sense data is usage/error statistics. See byte 2, bit 3 (SENSE 10) and format 6 (SENSE 25).
d. OS reissues the Start I/O.
e. OS writes the statistical record in SYS1.LOGREC.

ERROR DATA COLLECTION

Format

OS collects 24 sense bytes according to the method described below:

OS adds the following information:

Date and time
Device type
Program ID (name of the OS job)
Channel/unit address
Physical drive/CU ID
Volume ID (pack label)
Failing CCW
CSW
Last Seek address

OS formats the data and writes it to SYS1.LOGREC as an OBR outboard (logging mode) type record (MSG 40).

Method of Collection

When OS detects an I/O interrupt with Unit Check status, sense data is collected and analyzed by the system. An OBR record is written to SYS1.LOGREC following any occurrence of:

1. Equipment Check (soft, hard or permanent).
2. Bus out parity (soft or hard).
3. Permanent uncorrectable data check.

Note: This condition can occur when, because of data chaining, the system ERPs cannot compute the core location of the bad data in order to correct it by exclusive-ORing the pattern.

ENVIRONMENTAL DATA COLLECTION

Format

When a drive has entered logging mode, 24 sense bytes are collected as described below. They are identified by ERPs as environmental data by the presence of the usage/environmental data present bit (byte 2, bit 3) and not format 6.

OS adds the following information:

Date and time
Device type
Program ID
Channel/unit address
Physical drive/CU ID
Volume ID

OS formats the data and writes it to SYS1.LOGREC as an OBR outboard (logging mode) type record (MSG 40).

Logging Mode Entry Conditions

A drive must be in the logging mode for this data to be presented. This condition can be caused by either of the following:

1. Normal entry: occurs when a drive error (not usage) counter in control storage exceeds its predetermined threshold. The following events take place:
   a. The error/usage counters are read out and reset by the Sense command issued by OS following the next Start I/O attempt which addresses that drive. (See Statistical Data Collection, item 3.)
   b. Logging mode is entered for that drive.
2. Forced entry: occurs whenever the control unit CE panel Mode switch is not in the Normal position. All drives are forced into logging mode. This is done when the CE is checking out the subsystem with OLTs or when he wishes to collect additional data in SYS1.LOGREC to help him resolve an intermittent customer problem. For normal forced logging mode entry, the switch should be placed in the Forced Logging position.

Method of Collection — Control Unit

The CU collects 24 sense bytes of environmental data in its control storage when the following events occur:

1. Normal logging mode: logging mode data is collected whenever a drive in logging mode encounters an error of the same type that caused the CU to enter logging mode.
2. Forced logging mode: logging mode data is collected whenever a loggable error is detected on any drive.

Method of Collection — Operating System

OS collects 24 environmental data sense bytes as follows:

1. The next Start I/O addressing that drive is not executed. Instead, initial status presents Unit Check status.
2. OS issues a Sense command which transfers the sense data to the system for analysis. The Sense command resets the sense data following the transfer.
3. System ERPs determine that the data is environmental data (byte 2, bit 3).
4. OS reissues the Start I/O.
5. OS writes an OBR (logging mode) type of record into SYS1.LOGREC.

Termination of Logging Mode

1. Normal: logging mode terminates for either of the following:
   a. The drive has logged environmental sense data four times.
   b. A second drive enters logging mode before the first has finished. When this happens, logging mode is reset for the first drive. Only one drive at a time may be in logging mode.
2. Forced: when the control unit CE panel Mode switch is returned to Normal.

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CONSOLE ERROR MESSAGE ANALYSIS

BASIC CONSOLE ERROR MESSAGE FORMAT

	1		2		3		4		5		6		7		8
I E A 0 0 0 I	CUA(3)	,	ERROR DESCRIPTION(12)	,	CM(2)	,	CSW STAT(4)	,	SENSE DATA(4-48)	,	SEEK ADDRESS(12)	,	VOLUME ID(6)	,	JOB ID(8)

Notes on basic format:

1. The end of each field, except the last, is marked by a comma.
2. Sometimes a field is omitted. In this case it is delimited by its comma.
3. The message may consist of one or two lines.
   Each such line uses the basic format but prints different fields.

Notes on specific fields:

1. CUA = channel/unit address. Three characters.
2. Error descriptions applicable to type 3830-2 are: Cmd Reject, Int Reqd, Bus Out Ck, Equip Check, Data Check, Overrun, Intf Ctl Ck. Twelve characters.
3. CM = command code of last CCW executed. Two characters.
4. CSW status. First two hex characters = unit status; second two hex characters = channel status. Four characters.
5. Sense bytes printed in hex character pairs. Variable length.
6. Seek address = BBCCHH. Twelve characters.
7. Serial number of the volume mounted on the device. Six characters.
8. Job name. Eight characters.

ERROR MESSAGE CONTENT

Error Description	Fields Printed	Sense Bytes in Field 5
Intervention required	Line 1: 1,2,3,4,5, ,7,8 Line 2: None	0 - 4
Command Reject, Bus Out Parity, Overrun	Line 1: 1,2,3,4, , ,7,8 Line 2: 1, , , ,5,6	0 - 7
Equipment Check Data Check	Line 1: 1,2,3,4, , ,7,8 Line 2: 1, , , ,5	0 - 23

An error message has been printed on the console. The customer has directed your attention to it with a request for repair action. Refer to Basic Console Error Message Format for assistance in reading the message.

Read field 1 to verify that CUA is for type 3830-2 installed on the system

Read the error description from field 2 and follow corresponding directions

Intervention Required

One-line message. Device requiring intervention is specified in CUA field 1

Go to MLM for the device associated with address.

→ 3830-2 / 6 Device MLX Chart

Command Reject

Two-line message. Symptom code = '09YZ' where 'YZ' are hex digits of sense byte 7 in field 5 line 2.

This message is intended to signal programming errors; CE action is rarely required. If hardware difficulty is suspected, execute the diagnostic program most closely resembling the failing customer program.

Bus Out Parity

Two-line message. Symptom code = '0900'.

The maintenance procedure is outlined under symptom code '0900' with sense byte 0, bit 2 on.

Overrun

Two-line message. Symptom code = '0900'.

The maintenance procedure is outlined under symptom code '0900' with sense byte 0, bit 5 on.

Equipment Check

Two-line message.

Equipment Check may be written because of malfunctions described under sense formats 0, 1, 2 and 3.
For content of these formats refer to SENSE section.

Data Check

Two-line message.

Data Check is written for permanent, ECC-uncorrectable read errors under format 4. For content of this format refer to device MLM.

Check EREP history printouts and look for an "invalid track format" indication for this disk pack and seek address. If this condition occurred, suspect program problem with count field too large (writing into index).

Verify that the error is not due to a defective track by moving the failing disk pack to another physical drive. If a surface defect is suspected the operator can use utilities ATLAS or DASDI/DASDR to attempt data recovery and assign alternate surface for the defective track.

Go to MLM for the device associated with address.

→ 3830-2 / 8 Device MLX Chart

Interface Control Check

No error message.

An abnormal condition on the channel/CU interface has been detected by the channel.

In most cases involving the CU this is because of Disconnect In due to Check 1 error followed by Selective Reset from the channel. On subsequent selection, the CU will present Unit Check status (unless Check 1 is again present; in this case CC3 will result from selection) with sense information under format 3 leading to console message Equip Check.

→ START 30

Formats 0, 2, 3 → FSI 10

Format 1 → 3830-2 / 7 Device MLX Chart

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EREP SUMMARIES (OS)

Two summaries are produced for each device. (See MSG 10 for details of performance data collection.)

- Summary A shows how many records of the indicated types were found in SYS1.LOGREC data set.
- Summary B is generated from the statistical records identified in Summary A. It is an accumulation of the usage and error data collected by the control unit log.

Note: There may be two adjacent summary pages in the EREP output with the same physical channel unit address. In this case one of the summary sheets contains valid statistical summary information and the other summary sheet contains valid OBR error summary information. The sheet that shows a nonzero number of statistical records (right-hand column of Summary A) contains the valid statistical data for the device in Summary B. The other sheet contains valid OBR error summary data. Disregard Summary B on the latter.

1 DEVICE ID

The low-order digit of the physical channel unit address (Summary A) or the physical drive (Summary B) defines the physical drive according to the table:

Units Position of Address	Physical Drive
0	A
1	B
2	C
3	D
4	E
5	F
6	G
7	H

Note: If the CU has a Two Channel Switch or Two Channel Switch, Additional, feature, there may be other summaries for this physical device identified with the other channels to which it is connected. In this case, the summaries must be combined to get a complete summary for the device.

2 ERROR RECORD SUMMARY

3 LOGGING MODE ERROR RECORDS

When a disk drive error or usage counter (in control storage) exceeds its predetermined threshold (error counter), or overflows (usage counter), data is collected.

Usage/Error Threshold Values	
Bytes read	$2^{31}-1$
Access motions	$2^{15}-1$
Correctable Data Checks	512
Retry Data Checks	64
Seek Errors	8

The counts in the Environmental Record Summary are the number of detailed Unit Check records produced as a result of an abnormally high number of seek checks and data checks.

The frequency of data checks or seek checks is abnormally high if any of these counts are other than zero. The cause should be determined and appropriate maintenance action taken.

The actual number of seek checks and data checks can be determined from Summary B using the following relationship of fields:

Correctable Data Checks	=	Correctable Read Errors
Retry Data Checks	=	Retry Read Errors
Seek Checks	=	Access Errors

4 STATISTICAL INFORMATION

Totals shown here are the total statistical usage/error figures for this physical drive (151 in this example).

Total Accesses	–	a count of the total number of movable seeks issued to the drive.
Access Errors	–	a count of the number of seek incomplete errors detected by the drive plus the number of seek verification errors detected by the control unit.
Total Megabytes Read	–	a count of the number of megabytes read by the drive.
Retry Read Errors	–	the number of soft uncorrectable errors detected in any field (HA, count, key or data). They are recorded as format 4 Logging Mode records.
Correctable Read Errors	–	the number of correctable errors encountered in HA, count, key or data field. They are recorded as format 5 Logging Mode records.

SUMMARY A

```
SUMMARY OF I/O RECORDS   TYPE -OBR-   SOURCE - OUTBOARD   DEVICE TYPE 3330   MODEL-UNIVERSAL   SERIAL NO. 000000

            DAY YEAR     DAY YEAR
DATE RANGE- 204   71 TO  211   71

      1 PHYSICAL CHANNEL UNIT ADDRESS 000151    TOTAL NUMBER OF RECORDS 0033

 ERROR RECORD SUMMARY                        ENVIRONMENTAL RECORD SUMMARY

  BUS OUT PARITY        0000                 3 LOGGING MODE
                                                DATA CHECK
  EQUIPMENT CHECK                                 CORRECTABLE  0000
    CONTROL UNIT                                  RETRY        0000
      TEMPORARY         0000
      PERMANENT         0000                    SEEK CHECK     0001
    DRIVE
      TEMPORARY         0000                  STATISTICAL      0031
      PERMANENT         0000

 2 DATA CHK-PERMANENT   0001                  TOTAL            0032

  OVERRUN               0000

  INVALID TRACK FMT     0000

  TOTAL                 0001
```

SUMMARY B

```
SUMMARY OF I/O STATISTICAL RECORDS BY VOLUME ID                    DEVICE TYPE 3330

      1 PHYSICAL DRIVE        000151          TOTAL NUMBER OF RECORDS 0031

 VOLUME ID   TOTAL        ACCESS      TOTAL       RETRY       MEGABYTES    CORRECTABLE   MEGABYTES
             ACCESSES     ERRORS      MEGABYTES   READ        READ/RETRY   READ          READ/CORR
             (x1000)                  READ        ERRORS      ERROR        ERRORS        ERRORS

 SDA501      00042        00009       00410       N/A                      00010         00041
 111111      00074        00000       00704       N/A                      00021         00033
 SYS50Y      00000        00000       00009       N/A                      N/A
 222222      00000        00000       00000       N/A                      N/A

 TOTALS      00116        00009       01124       00000       00000        00031         00036

TOTAL OVERRUNS CHNL A                  TOTAL OVERRUNS CHNL B
 1            COMMAND   00000                      COMMAND   00000
              DATA      00000                      DATA      00000
```


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EREP UNIT CHECK RECORD (OS)

❶ ENVIRONMENTAL INFORMATION

System supplied information is provided at the top of each page of the EREP printout of a device Unit Check record. The information describes the operating environment at the time of the failure. Errors recorded by System/360 or by a release of OS below release 21.0 may not contain valid information in the Model, Serial Number and OS Release fields.

Note: The Job Identity, which indicates a means of recreating the failure, may contain zeros if a system task was in operation.

❷ OBR RECORD CONVERTED TO THE STANDARD FORMAT

This message will appear in all printouts of Unit Check records created by a system below OS Release 21.0.

❸ PRIMARY CHANNEL UNIT ADDRESS

This is the primary physical address of the device and is equivalent to the physical channel unit address or physical drive shown on the summary sheet (MSG 30).

❹ ALTERNATE CHANNEL UNIT ADDRESS

This is the actual logical address path over which the error occurred. If the high order (channel) digit is zero, as shown in this example, disregard the channel digit. If it is other than zero, it indicates the channel on which the error actually occurred.

❺ VOLUME LABEL

The Volume Label printed is the Volume Label of the pack being used at the time of the failure. This information is provided as an aid in determining whether the error was caused by a hardware failure or by a pack problem.

❻ KEYWORDS

Keyword error description corresponds to that given in Summary A on MSG 30.

❼ ERROR SYMPTOM CODE

The error symptom code is taken from bytes 22-23 of the sense data. The maintenance analysis procedure is obtained by using the error symptom code as entry into the Fault Symptom Index starting on FSI 10.

❽ FAILING CCW, CSW, LAST SEEK ADDRESS

This information is provided to further define conditions at the time of the failure.

Note: This information is invalid when it appears on the printout of Logging Mode errors.

❾ SENSE BYTE DATA

In this example, this field indicates that the detailed sense printout is of a format 0 Unit Check record.

❿ DETAILED SENSE BYTE PRINTOUT

Each sense byte which contains significant information is expanded to show the bits that are on. The bit definition is printed to the left of the bit. The hex value of the byte is printed to the right of the byte number.

Bytes 0-7

Bytes 0-7 in sense formats 0-5 have common definitions:

- Bytes 0-2 describe the Unit Check condition.
- Byte 3 contains the restart command.
- Bytes 4-6 describe the pack and drive address.
- Byte 7 contains the format number and message code.

Format 0 Sense Data (Message Only)

Bytes 8-21 contain zeros. Format 0 sense contains message information only.

Format 2 Sense Data (Control Unit Errors)

Bytes 8-21 contain detailed error information which should not be used unless the error symptom code failed to point to the maintenance analysis procedure.

Format 3 Sense Data (Selective Reset Errors)

Bytes 8-21 contain detailed error information which should not be used unless the error symptom code failed to point to the maintenance analysis procedure.

⓫ HEX DUMP OF RECORD

This is the raw form of the data comprising the Unit Check EREP printout.

```
---RECORD ENTRY TYPE - UNIT CHECK     SOURCE - OUTBOARD                MODEL- 0145        SERIAL NO. 010613
                                                                                                                  ❶
                        DAY YEAR                        HH MM SS.TH                      JOB IDENTITY LJOB
                  DATE- 159   72                  TIME  20 25 08 08                                D3D1D6C240404040

OBR RECORD CONVERTED TO THE STANDARD FORMAT ❷

 DEVICE TYPE                          3330
 PHYSICAL   CHANNEL UNIT ADDRESS      000256 ❸
 LOGICAL    CHANNEL UNIT ADDRESS      000251 ❹
 PHYSICAL DRIVE                       NONE
 PHYSICAL CONTROL UNIT                1
 VOLUME LABEL                         MIDI01 ❺

 OVER RUN ❻
ERROR SYMPTOM CODE- 0000 ❼
                  CC   CA   FL     CT                          K    CA   US CS  CT
FAILING CCW       1A 0529F8  40 00 0005          CSW           00 0505B0 0E 00 0000   ❽

                  M  B B  C C  H H  R
LAST SEEK ADDRESS- 00 0000 0002 0000 00

SENSE BYTE DATA-  FORMAT 0 ❾

  BYTE 0   04     BYTE 1   00     BYTE 2   00     BYTE 3   06     BYTE 4   7E     BYTE 5   00     BYTE 6   00     BYTE 7   00
----------UNIT CHECK DESCRIPTION----------  RESTART CMND   PHYSICAL ID    CYL(1 TO 128)--HEAD---------  FORMAT/MSG

COMMAND REJ 0  PERM ERROR  0                0   00000110   CU/CTRLR    0  CYL 128    0  REVERSE    0  FORMAT  8   0
INTERVN REQ 0  INV TRK EMT 0  CORRECTABLE   0              CU/CTRLR    1  CYL  64    0  CYL 256    0  FORMAT  4   0
BUS OUT PAR 0  END OF CYL  0                0              DRIVE 3/6   1  CYL  32    0  DIF 256    0  FORMAT  2   0
EQUIPMNT CK 0              0  ENV DATA PR   0              DRIVE 3/6   1  CYL  16    0  HEAD 16    0  FORMAT  1   0
DATA CHECK  0  NO REC FND  0                0              DRIVE 3/6   1  CYL   8    0  HEAD  8    0  MESSAGE 8   0
OVERRUN     1  FILE PROTCT 0                0              DRIVE 3/6   1  CYL   4    0  HEAD  4    0  MESSAGE 4   0
            0  WRT INHIBIT 0                0              DRIVE 3/6   1  CYL   2    0  HEAD  2    0  MESSAGE 2   0
            0  OP INCOMPLT 0                0              DRIVE 3/6   0  CYL   1    0  HEAD  1    0  MESSAGE 1   0
                                                                                                                  ❿

  BYTE 8   00     BYTE 9   00     BYTE 10  00     BYTE 11  00     BYTE 12  00     BYTE 13  00     BYTE 14  00     BYTE 15  00
 00000000        00000000        00000000        00000000        00000000        00000000        00000000        00000000

  BYTE 16  00     BYTE 17  00     BYTE 18  00     BYTE 19  00     BYTE 20  00     BYTE 21  00     BYTE 22  00     BYTE 23  00
                                                                                                -----ERROR SYMPTOM CODE-----
 00000000        00000000        00000000        00000000        00000000        00000000        00000000        00000000

 HEX DUMP OF RECORD
 HEADER     30150800     00000000     0072159F     20250808     00010613     014500C0
                                                                                                                  ⓫
      0000  D3D1D6C2     40404040     1A0529F8     40000005     000505B0     0E000000     03000251     30702008
      0020  00000256     0C000018     D4C9C4C9     F0F10000     00000000     02000000     00000002     00000000
      0040  0400C004     7E000000     00000000     00000000     00000000     00000000
```


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Storage Multiple Read Error
Address Bus 8-15 Parity Error
ECC Logic Error
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Storage Display

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ACR Sync, Stop and Recycle
Sw, Sync, or Stop

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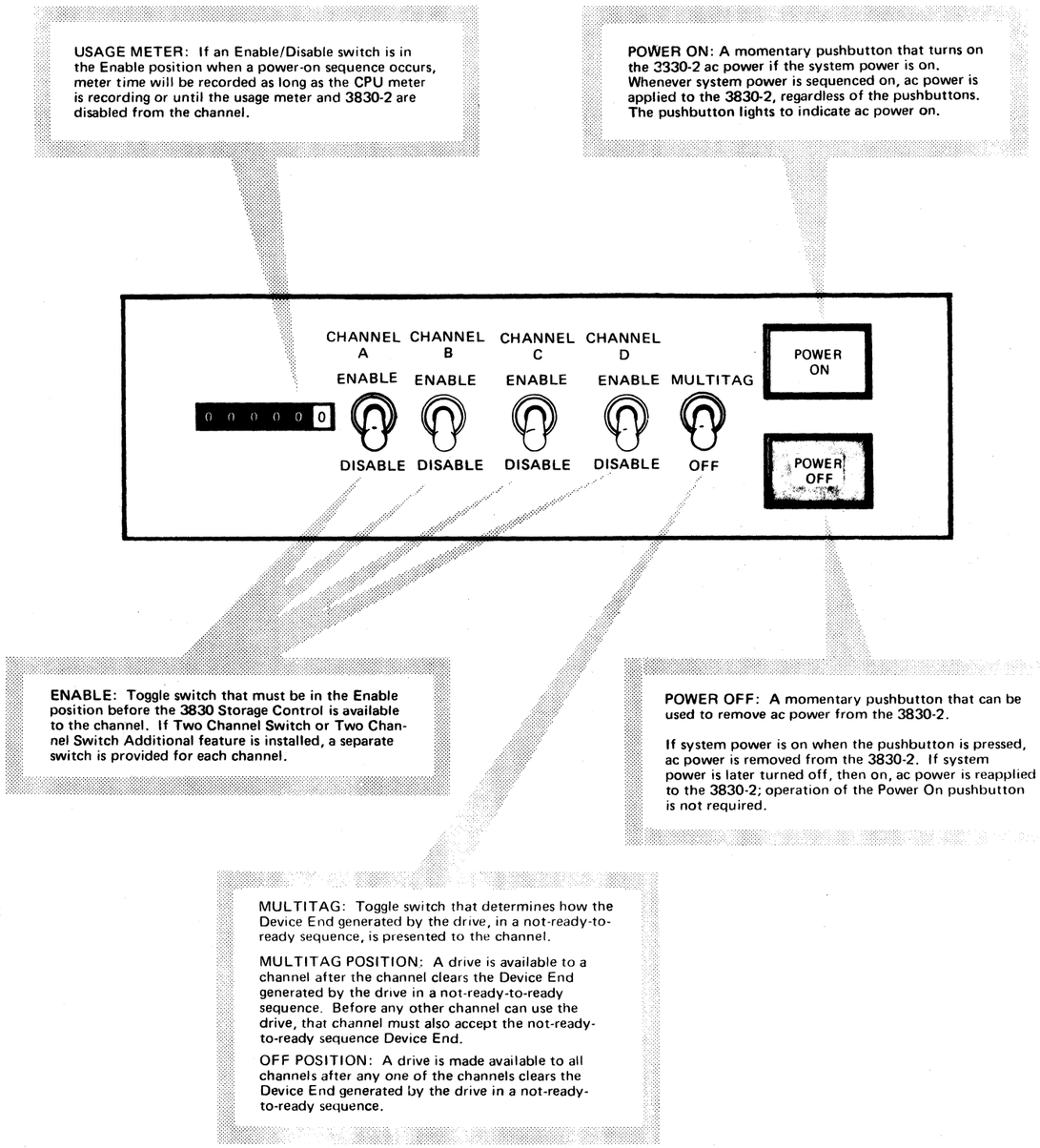
POWER SEQUENCE PANEL



CE PANEL (Part 1 of 2)

- Description of CE Panel controls and indicators
- For CE Panel operations see PANEL 15

MPL FILE

POWER ON INDICATOR
Indicates that power is applied to the MPL file and the disk is rotating.

SEEK IN/SEEK OUT LOAD HEAD SWITCH
Three position toggle switch, that loads the read head and moves the head one track towards center of disk (Seek In) or one track away from center of disk (Seek Out). (CE Modes)

IMPL SWITCH
Initiates an initial microprogram load operation. (Control unit must be stopped, reset, and in a CE Mode).

ADDRESS/CHECK/PROGRAM DISPLAY INDICATORS
Displays information selected by Enter/Display switch. Displays addresses for alter, display, and address compare functions. Also displays diagnostic messages.

REGISTER/STORAGE DISPLAY INDICATORS
Displays information selected by Enter/Display switch.

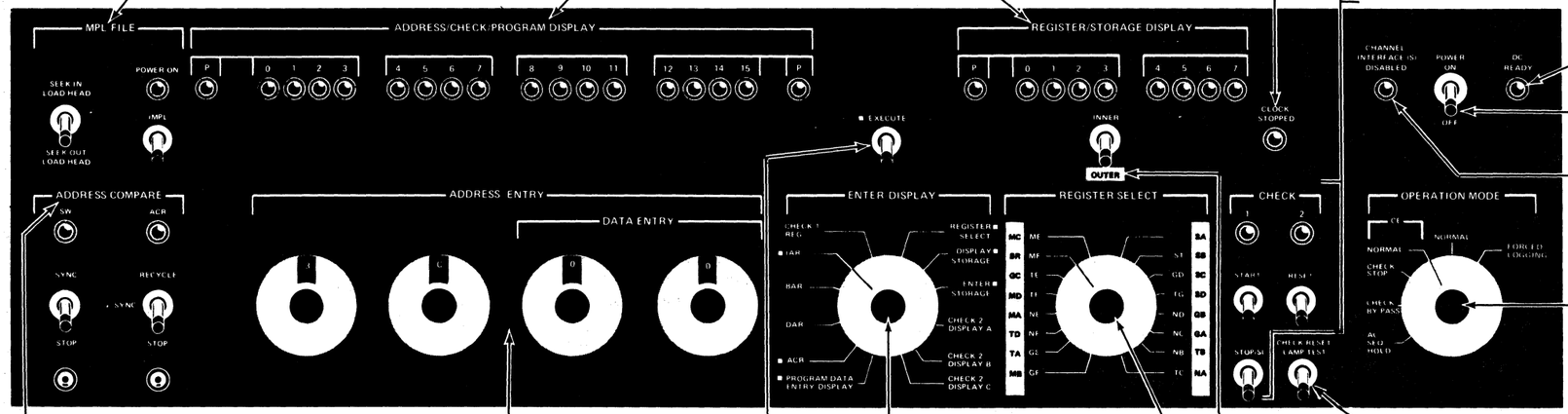
CLOCK STOPPED INDICATOR
Indicates that storage control unit clock is stopped.

CHECK INDICATORS
Indicate when a Check 1 or Check 2 error is detected. (See PANEL 40,50.)

START SWITCH
Executes the microprogram starting with the instruction specified by the IAR. (CE Modes)

RESET SWITCH
Activates all storage control unit reset lines. (CE Modes)

STOP/SI SWITCH
Control unit running: Stops control unit (CE Modes).
Control unit stopped: Executes one microprogram instruction (CE Modes).



DC READY INDICATOR
Indicates that storage control unit power sequence is complete.

POWER SWITCH
Two position spring loaded switch, that controls power on or off in CE modes.

CHANNEL INTERFACE(S) DISABLED INDICATOR
Indicates when the channel interface drivers are degated. For two or two channel switch additional features, all channel interfaces must be degated.

OPERATION MODE SWITCH

ADDRESS/DATA ENTRY SWITCHES
Enter addresses and/or data for microprogram communication, control storage locations, address compare functions, and registers.

ADDRESS COMPARE

Address Entry Switches → COMPARE

SW INDICATOR
Indicates equal compare. Latched until reset with Check Reset Lamp Test switch.

SYNC/STOP SWITCH
Sync position: Emits 40 nsec pulse at sync hub (located below switch) for each equal compare. (See Note 1.)
Stop position: Microprogram halts before executing instruction at address providing equal compare. (CE Modes)

ADDRESS BUS (Control Storage)

Address Compare Register (ACR) → COMPARE

ACR INDICATOR
Indicates equal compare. Latched until reset with Check Reset Lamp Test switch.

RECYCLE/SYNC/STOP SWITCH
Recycle position: Emits 40 nsec pulse at sync hub (located below switch) and branches to instruction address contained in Address Entry switches. (See Note 1.)
Microprogram continues to run. (CE Modes)
Sync position: Emits 40 nsec pulse at sync hub (located below switch) for each equal compare. (See Note 1.)
Stop position: Microprogram halts before executing instruction at address providing equal compare. (CE Modes)

ADDRESS BUS (Control Storage)

■ EXECUTE SWITCH
Used with Enter/Display switch to activate an alter or display cycle. Also used to enter parameters and execute microprograms.

ENTER/DISPLAY SWITCH
Selects registers, control storage locations, or program data for display or alteration:

SWITCH POSITION	FUNCTION ALTER	FUNCTION DISPLAY	INDICATORS USED
CHECK 1 REG		X	ADDR/CHK/PROG DISPLAY
■ IAR	X	X	
BAR		X	
DAR		X	
■ ACR	X	X	
■ PGM DATA ENTRY/DISPLAY	X	X	
■ REGISTER SELECT	X	X	REG/STOR DISPLAY
■ DISPLAY STORAGE		X	
■ ENTER STORAGE	X		
CHECK 2 A	(Check 2 POSITIONS NOT USED)		
CHECK 2 B			
CHECK 2 C			

← ■ *Indicates that Execute switch is used with this switch position.*

INNER/OUTER SWITCH
Selects one of two groups of registers for Register Select switch.

REGISTER SELECT SWITCH
Selects one of 31 general purpose registers for display or alteration. Used with Inner/Outer switch and Enter/Display switch.

Note 1: As an aid to troubleshooting in the device, sync pulses can be transmitted through the control interface cable to the device via the CE Communication Out driver. See CTL-I 10 for procedure.

CE MODES CAN AFFECT CUSTOMER OPERATION USE CAUTION

EFFECT ON 3830/ CE PANEL		MODES: NORMAL	FORCED LOGGING	CE: NORMAL	CE: CHECK STOP	CE: CHECK BY PASS	CE: AC SEQ HOLD
Address compare indicators and sync hubs active		YES	YES	YES	YES	YES	This Position Not Needed. Operates As in CE Check Stop Mode
CHECK RESET LAMP TEST SWITCH	Resets Addr. Comp Indicators	YES	YES	YES	YES	YES	
	Resets Error Latches	NO	NO	YES	YES	YES	
	Tests Panel Lamps	YES	YES	YES	YES	YES	
All panel controls/functions allowed		NO	NO	YES	YES	YES	
Machine stops at end of error (CHK 1) cycle		YES	YES*	YES	YES	NO	
Machine stops at end of error (CHK 2) cycle		NO	NO	NO	YES	NO	
All errors (CHK 1 and CHK 2) ignored		NO	NO	NO	NO	YES	
Selective Reset from system channel inhibited		NO	NO	YES	YES	YES	
PROGRAM DATA ENTRY/ DISPLAY (communication) allowed		NO	YES	YES	YES	YES	

*If Special Op 28 was issued previously, a selective reset will occur in Forced Logging mode and the clock will restart.

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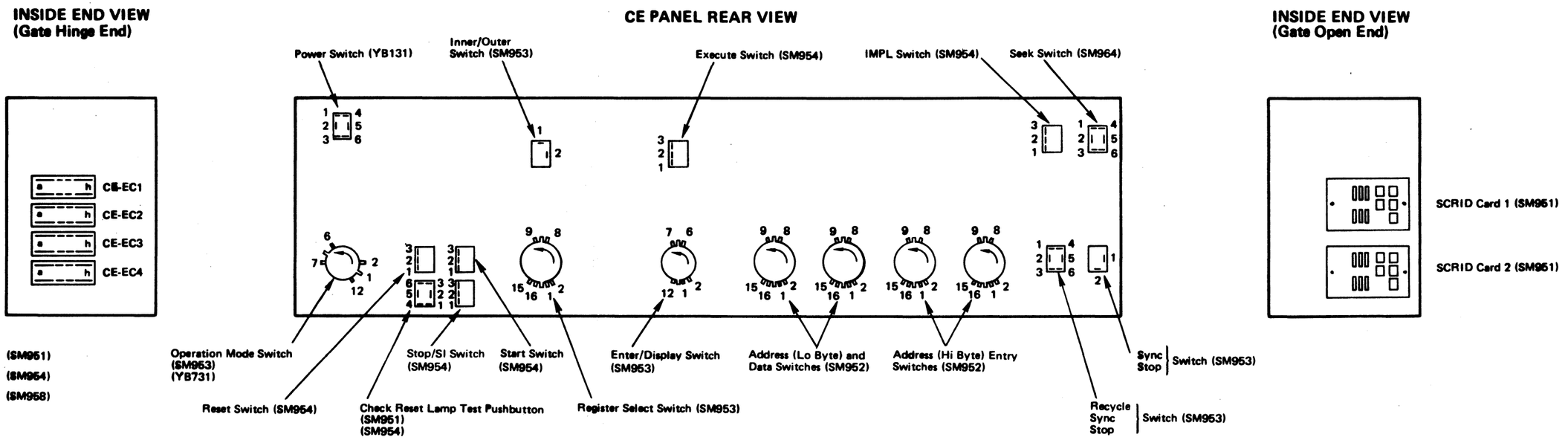
CE PANEL (Part 2 of 2)



Note: See SM958 for detail of rotary switches

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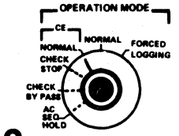
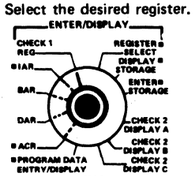
CE PANEL OPERATIONS (Part 1 of 2)

REGISTER DISPLAY

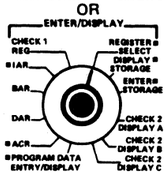
1 Select a CE mode and stop the machine.

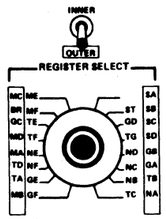


2 Select the desired register.



OR





CAUTION

- *Any mode other than normal or forced logging may affect customer data when operating in modes other than normal or forced logging.*
- *All channels must be disabled and Channel Disabled indicator on.*
- *Or, customer data packs must be removed or drives containing customer packs turned off.*

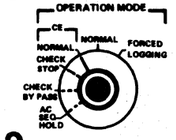
The Enter/Display switch permits selection and display, in the Address/Check/Program Display lights, of the IAR, BAR, DAR, or ACR register. See PANEL 100 for circuit description.

To select a general purpose register, place the Enter/Display switch to Register Select; then make a selection with the Inner/Outer and Register Select switches. The display is in the Register/Storage display lights. See PANEL 100 for circuit description. The TF Register can be altered or displayed as a normal general purpose register.

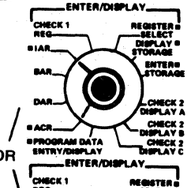
To alter or display the MF, NF, and GF Registers, the TF Register must be set to '00'. 'F' Registers are a special feature. Refer to INTR 005 and MIC 40.

REGISTER ALTER

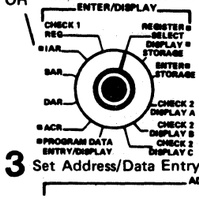
1 Select a CE mode and stop the machine. Operate Reset switch.

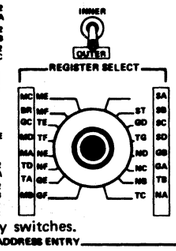


2 Select the desired register.



OR

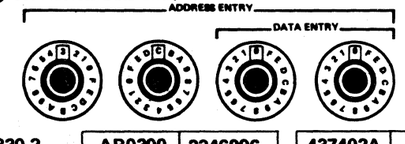




The Enter/Display switch provides selection of registers IAR and ACR. To select a general purpose register, place the Enter/Display switch to Register Select; then make a selection with the Inner/Outer and Register Select switches. See PANEL 105, 110. The TF Register can be altered or displayed as a normal general purpose register.

To alter or display the MF, NF, and GF Registers, the TF Register must be set to '00'. 'F' Registers are a special feature. Refer to INTR 005 and MIC 40.

3 Set Address/Data Entry switches.



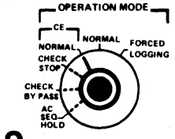
The desired data should be set with the Data Entry switches.

4 Operate Execute.

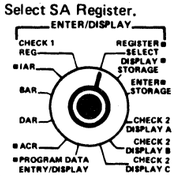
The data set in the Data Entry switches is loaded into the selected register, and displayed for checking.

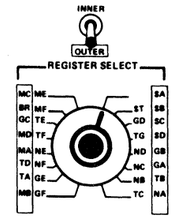
STORAGE ALTER

1 Select a CE mode and stop the machine. Operate Reset switch.



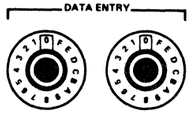
2 Select SA Register.





Set Inner/Outer switch to Outer position. A byte must be loaded into each storage register (SA, SB, SC, SD).

3 Set Data Entry switches.



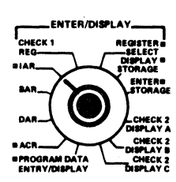
The desired data is entered in these two switches.

4 Operate Execute.

The Data Entry switches are loaded into the selected register.

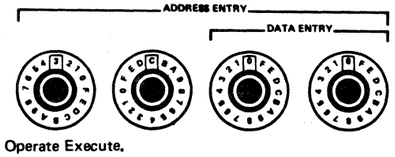
5 Repeat steps 2, 3, and 4 for SB, SC, and SD registers.

6 Select IAR.



IAR must be loaded with the desired control storage address.

7 Set Address/Data Entry switches.



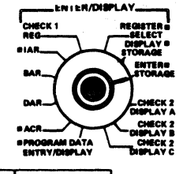
The desired address is entered into these switches. The low-order Data Entry switch must be on a word boundary: 0, 4, 8, or C.

CAUTION
An invalid parity can be loaded if an even boundary is not entered.

8 Operate Execute.

IAR is loaded with the Address/Data Entry switches.

9 Select Enter Storage.

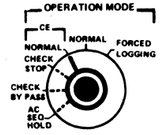


10 Operate Execute.

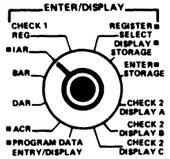
The selected storage location is loaded with contents of SA, SB, SC, and SD

STORAGE DISPLAY

1 Select a CE mode and stop the machine. Operate Reset switch.

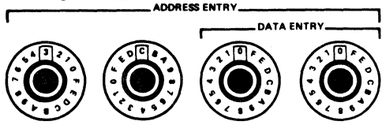


2 Select IAR.



The IAR must be loaded with the storage location to be displayed.

3 Set storage address.

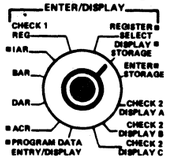


The desired storage location must be selected. The low-order Data Entry switch must be on an even-word boundary: 0, 4, 8, or C.

4 Operate Execute.

The IAR is loaded with address of desired storage location.

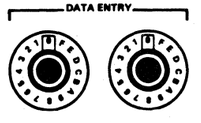
5 Select Display Storage.



6 Operate Execute.

Byte 0 of the word fetched is displayed in the Register/Storage Indicators after the Execute switch is operated.

7 Display any of four bytes with low-order Data Entry switch.



Four bytes (0-3) are fetched from control storage. The low-order Data Entry switch position determines which byte is displayed.

Byte Displayed In Register/Storage Indicators	Low Order Data Entry Switch
0	0, 4, 8, or C
1	1, 5, 9, or D
2	2, 6, A, or E
3	3, 7, B, or F

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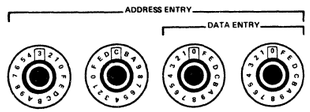
CE PANEL OPERATIONS (Part 2 of 2)

CAUTION
- *Any mode other than normal or forced logging may affect customer data when operating in modes other than normal or forced logging.*
- *All channels must be disabled and Channel Disabled indicator on.*
- *Or, customer data packs must be removed or drives containing customer packs turned off.*

ADDRESS COMPARE

SW Address Compare Sync or Stop

1 Set address of desired instruction in Address/Data Entry switches.



The address compare is made on the storage address bus. The bus can have either an instruction address or a data address.

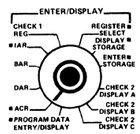
2 Set SW to Sync or Stop.

If Sync is selected, machine provides a 40 ns pulse at SW sync hub when a compare is made between address and the Address/Data Entry switches. (See Note 1.) If Stop is selected, and machine is in one of the three CE modes, machine stops before executing the instruction at the address that compares with Address/Data Entry switches.

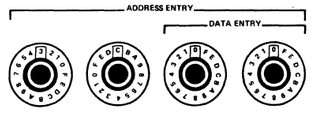
3 Place machine in run mode.

ACR Address Compare Sync or Stop

1 Select ACR.



2 Set address of desired instruction in Address/Data Entry switches.



The address compare is made on the storage address bus. The bus can have either an instruction address or a data address.

3 Operate Execute.

The desired address is loaded into the ACR.

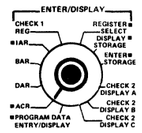
4 Set Mode switch to desired operation.

5 Set ACR switch to Sync or Stop.

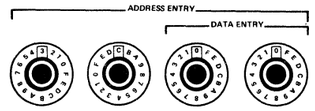
If Sync is selected, machine provides a 40 ns pulse at ACR sync hub when a compare is made between instruction address that compares with ACR. (See Note 1.)
If Stop is selected, and the machine is in one of the three CE modes, machine stops at instruction address that compares with ACR.
The instruction has not been executed.

Address Compare Recycle

1 Select ACR.



2 Set Address/Data Entry switches with address of last instruction to be executed.

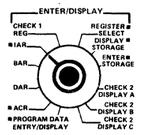


This address is determined from the instruction loop.

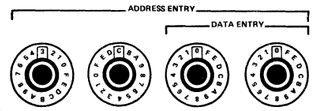
3 Operate Execute.

The desired address is loaded into the ACR.

4 Select IAR.



5 Set Address/Data Entry switches with starting instruction address.



6 Operate Execute.

The starting address is loaded into the IAR. The switches should remain at this setting to maintain the instruction loop.

7 Set desired operation.

8 Set Recycle.

9 Operate Start or SI.

Machine will execute a sequence of instructions starting with the address loaded into IAR. When the ACR compares with an address in the sequence, the machine branches to the address contained in the Address/Data Entry switches. The sequence of instructions starting with the address in the switches is then executed until another address compare (with ACR) occurs. The machine again branches to the address in the Address/Data Entry switches. After loading IAR (original start address), the Address/Data Entry switches can be changed. This results in a new "branch to" address.

POWER OFF PROCEDURE

1 Vary individual drive offline.

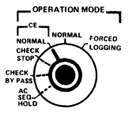
2 Set storage control meter switch to Disable.

This switch is located on the storage control power sequence panel.

3 Wait for the channel interface disabled indication.

For two channel switch or two channel switch additional, feature, all interfaces must be disabled to light indicator.

4 Place CU in CE Normal mode.



5 Place Power On/Off to Off.

Note 1: As an aid to troubleshooting in the device, sync pulses can be transmitted through the control interface cable to the device via the CE Communication Out driver. See CTL-I 10 for procedure.

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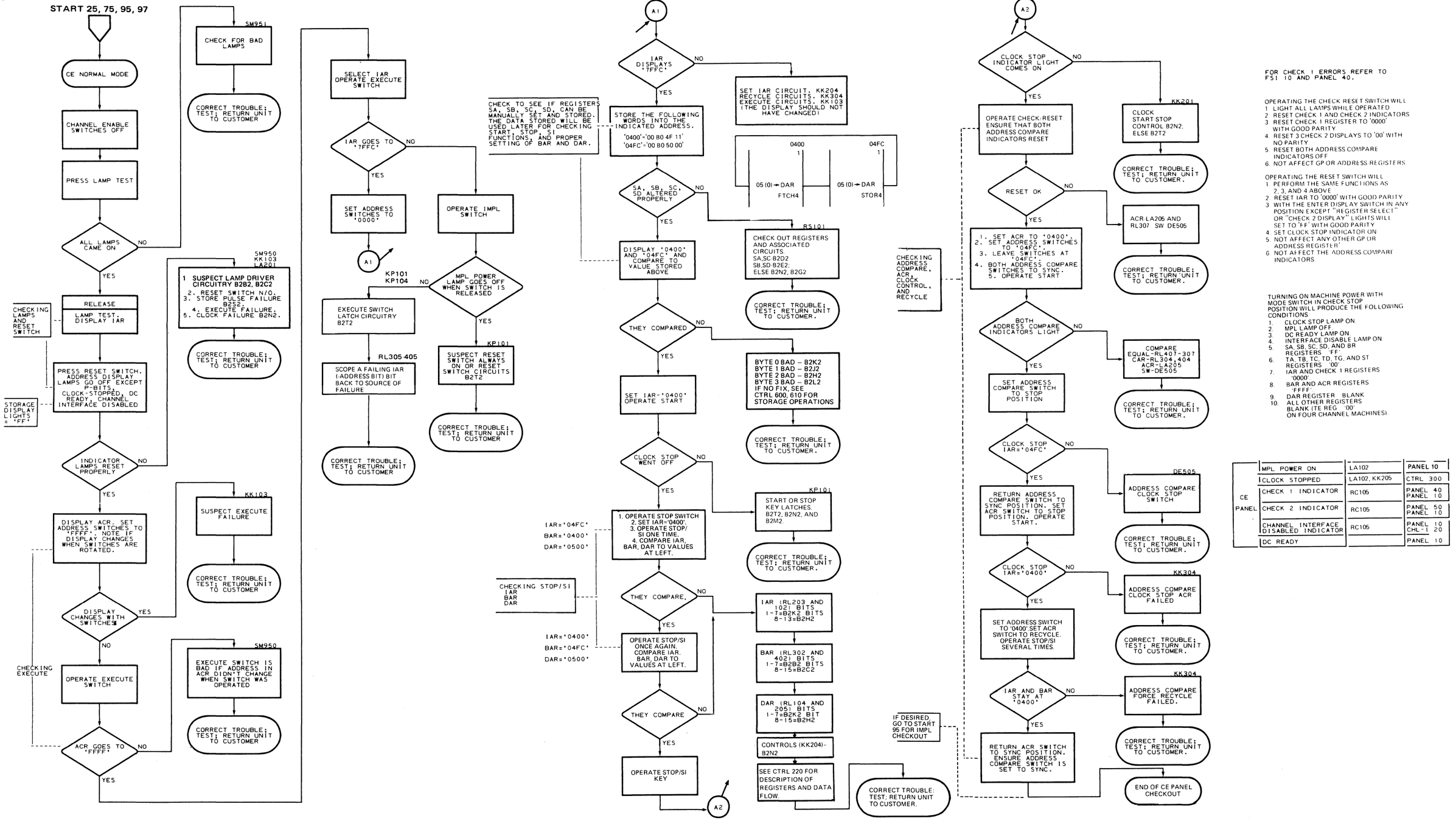
CE PANEL CHECKOUT

REFER TO CLOCK STOP ECD–START 95-97, CTRL 40, KK201



FOR CHECK 1 ERRORS REFER TO FSI 10 AND PANEL 40.

OPERATING THE CHECK RESET SWITCH WILL
1. LIGHT ALL LAMPS WHILE OPERATED
2. RESET CHECK 1 AND CHECK 2 INDICATORS
3. RESET CHECK 1 REGISTER TO '0000' WITH GOOD PARITY
4. RESET 3 CHECK 2 DISPLAYS TO '00' WITH NO PARITY
5. RESET BOTH ADDRESS COMPARE INDICATORS OFF
6. NOT AFFECT GP OR ADDRESS REGISTERS

OPERATING THE RESET SWITCH WILL
1. PERFORM THE SAME FUNCTIONS AS 2, 3, AND 4 ABOVE
2. RESET IAR TO '0000' WITH GOOD PARITY
3. WITH THE ENTER DISPLAY SWITCH IN ANY POSITION EXCEPT "REGISTER SELECT" ON "CHECK 2 DISPLAY" LIGHTS WILL SET TO 'FF' WITH GOOD PARITY
4. SET CLOCK STOP INDICATOR ON
5. NOT AFFECT ANY OTHER GP OR ADDRESS REGISTER
6. NOT AFFECT THE ADDRESS COMPARE INDICATORS

TURNING ON MACHINE POWER WITH MODE SWITCH IN CHECK STOP POSITION WILL PRODUCE THE FOLLOWING CONDITIONS
1. CLOCK STOP LAMP ON.
2. MPL LAMP OFF.
3. DC READY LAMP ON.
4. INTERFACE DISABLE LAMP ON.
5. SA, SB, SC, SD, AND BR REGISTERS 'FF'.
6. TA, TB, TC, TD, TG, AND ST REGISTERS '00'.
7. IAR AND CHECK 1 REGISTERS '0000'.
8. BAR AND ACR REGISTERS 'FFFF'.
9. DAR REGISTER BLANK.
10. ALL OTHER REGISTERS BLANK (TE REG '00' ON FOUR CHANNEL MACHINES).

CE PANEL	MPL POWER ON	LA102	PANEL 10
	CLOCK STOPPED	LA102, KK205	CTRL 300
	CHECK 1 INDICATOR	RC105	PANEL 40 PANEL 10
	CHECK 2 INDICATOR	RC105	PANEL 50 PANEL 10
	CHANNEL INTERFACE DISABLED INDICATOR	RC105	PANEL 10 CHL-1 20
	DC READY		PANEL 10

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CHECK 1 ERROR COLLECTION (Part 1 of 2)

Check 1 errors prevent the microprogram from running correctly. Check 1 errors:

- Stop CU clock
- Are stored in Check 1 register along with:
  1. MPL File errors
  2. Control Storage errors
- Are indicated by Check 1 lamp on CE panel

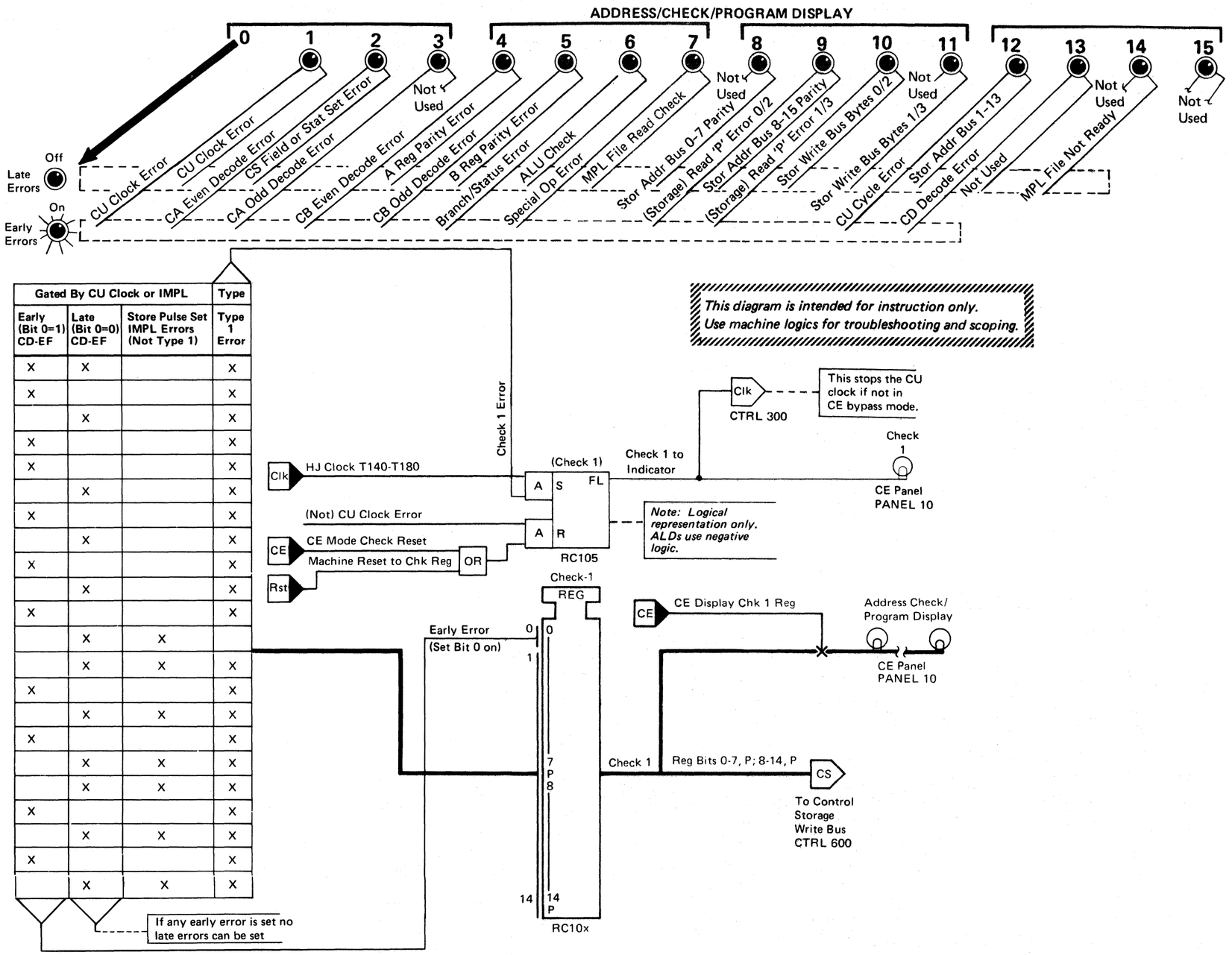
Check 1 register contents:

- Can be read out to Address/Check/Program display on CE panel (see PANEL 15).
- Are written at control storage location '064A' and '064B' after Selective Reset is received from the channel.

FOR MAINTENANCE SEE FSI SECTION (BEGINS ON FSI 30)

Keyed to text on PANEL 41	Error Name	Error Condition Diagram (ECD)	ALD Page	Gated By CU Clock or IMPL: Early (Bit 0=1) CD-EF	Gated By CU Clock or IMPL: Late (Bit 0=0) CD-EF	Gated By CU Clock or IMPL: Store Pulse Set IMPL Errors (Not Type 1)	Type 1 Error
1	CU Clock Error	CTRL 40	KK201	X	X		X
2	CA Even Decode Error	CTRL 20	RL208	X			X
	CS Decode Error ST Register Set Error	CTRL 30	DE201		X		X
3	CA Odd Decode Error	CTRL 20	RL208	X			X
4	CB Even Decode Error	CTRL 25	DE504	X			X
	A Reg Parity Error	CTRL 35	RA201		X		X
5	CB Odd Decode Error	CTRL 25	DE504	X			X
	B Reg Parity Error	CTRL 35	RA202		X		X
6	Branch/Status Error	CTRL 45	DE306	X			X
	ALU Check	CTRL 60	RA303		X		X
7	Special Operation Error	CTRL 40	DE403	X			X
	MPL File Read Check (23FD Parity)	MPL 295	LA306		X	X	
8	Storage Address Bus 0-7 Parity Error	CTRL 50	RL208		X	X	X
9	Storage Read 'P' Error 0/2	CTRL 610	SW535	X			X
	Storage Address Bus 8-15 Parity Error	CTRL 50	RL104		X	X	X
10	Storage Read 'P' Error 1/3	CTRL 610	SW535	X			X
	Storage Write Bus Error–Bytes 0/2	CTRL 610	SW455		X	X	X
11	Storage Write Bus Error–Bytes 1/3	CTRL 610	SW455		X	X	X
12	CU Cycle Control Error	CTRL 40	KK301	X			X
	Storage Addr Bus 1-13 Error	CTRL 620	SW451		X	X	X
13	CD Decode Error	CTRL 30	DE107	X			X
14	MPL File Not Ready	MPL 295	LA204		X	X	X

If any early error is set no late errors can be set



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CHECK 1 ERROR COLLECTION (Page 2 of 2)

1 CU CLOCK ERROR
(CTRL 40)

Generated by incorrect sequence in clock timing.

1. Turns on Check register bit 1, and error latch.
2. Stops CU clock.

2 CA EVEN DECODE ERROR
(CTRL 20)

Error conditions are generated by a check of even CA decodes.

1. Even numbered register selected on an odd CA decode.
2. Even numbered register selected on CA=0.
3. None, or an even number of even registers selected on an even CA decode (CA≠0).

CS FIELD OR STAT SET ERROR
(CTRL 30)

The individual bits of the status (ST) register are set or reset according to decodes of the CS field. The set/reset circuits for status bits are duplicated. A Status Set error is indicated by:

1. The predicted parity of the Status set/reset circuits does not compare with the actual parity of the sets to the ST register.
2. Parity error occurred on the CS field input to the CS decoder.
3. Even number of CS decodes was detected.
4. The microprogram attempted to set or reset the Status register simultaneously by the CS field and by CD decode.
5. The microprogram set or reset Status register bit 4 simultaneously with the user.
6. The microprogram set or reset status register bit 3 and simultaneously specified ALU operations 4, 5, or 6 (Carry Line active).

3 CA ODD DECODE ERROR
(CTRL 20)

Generated by a check of the odd decodes.

1. Odd numbered register selected on an even CA decode.
2. None, or an even number of odd registers selected on an odd CA decode.

4 CB EVEN DECODE ERROR
(CTRL 25)

Generated by a check of the even decodes.

1. Even numbered register selected on an odd CB decode.
2. Even numbered register selected on CB=16 (no register selected).
3. None, or an even number of even registers selected on an even CB decode (CB≠16).
4. An unplugged optional even register selected by an even CB decode.

A-REGISTER PARITY ERROR
(CTRL 35)

The A-register is checked for odd parity.

5 CB ODD DECODE ERROR
(CTRL 25)

Generated by a check of the odd decodes.

1. Odd numbered register selected on an even CB decode.
2. None, or an even number of odd registers was selected on an odd CB decode.
3. Unplugged optional odd register selected by an odd CB decode.

B-REGISTER PARITY ERROR
(CTRL 35)

The B-register is checked for odd parity.

6 BRANCH/STATUS ERROR
(CTRL 45)

The Branch error is turned on under four conditions.

1. ST Reg Parity Error. The ST register circuits are duplicated and compared.
2. Read byte 3 (CH, CL control) is checked for parity.
3. CH branch decode error. CH decode circuit is duplicated and compared.
4. CL branch decode error. CL decode circuit is duplicated and compared.

ALU CHECK
(CTRL 60)

The ALU circuit is checked for:

1. D-Bus parity checked for odd.
2. Op decode input parity, outputs, and carry in-carry out controls do not match.
3. D-Bus equal zero and duplicate circuits do not match.

7 SPECIAL OPERATION ERROR
(CTRL 40)

None, or an even number of special operations are decoded while in format F mode.

MPL FILE READ CHECK
(MPL 295)

Parity check of MPL byte assembly register.

8 STORAGE ADDRESS BUS 0-7 PARITY ERROR
(CTRL 50)

The address bus high order bits are checked for odd parity. Address may be from IAR, DAR, or IMPL circuits. Checked in CU.

9 (STORAGE) READ 'P' ERROR 0/2
(CTRL 65)

Control storage detected even parity on read, byte 0 or 2.

STORAGE ADDRESS BUS 8-15 PARITY ERROR
(CTRL 50)

The address bus low order bits are checked for odd parity. Address may be from IAR, DAR, or IMPL circuits. Checked in CU.

10 (STORAGE) READ 'P' ERROR 1/3
(CTRL 65)

Control storage detect even parity on read, byte 1 or 3.

STORAGE WRITE BUS ERROR BYTES 0/2
(CTRL 610)

Control storage write bus bytes 0 and 2 are checked on all store cycles for odd parity.

11 STORAGE WRITE BUS ERROR BYTES 1/3
(CTRL 610)

Control storage write bus bytes 1 and 3 are checked on all store cycles for odd parity.

12 CU CYCLE CONTROL ERROR
(CTRL 40)

Cycle control latches are checked for none, 2, or 4 on.

ADDRESS BUS 1-13 ERROR
(CTRL 610)

Incorrect parity in storage address bits 1-7, P or 8-13, P (addresses '0000'-'7FFF'). Bits are checked on the addressed array card within control storage.

13 CD DECODE ERROR
(CTRL 30)

Note: Error occurred on cycle previous to its detection

Generated by a check of the CD decodes.

1. Even inputs to the CD decoder.
2. The predicted parity of the CD decode gate lines does not compare with actual parity of the sets to the registers.
3. A register selected by CD decode was also selected by external lines.

14 MPL FILE NOT READY
(MPL 295)

MPL file cannot do an IMPL or read operation.

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CHECK 2 ERROR COLLECTION (Part 1 of 2)

- Check 2 circuits indicate failures in:
  Control interface
  Channel interface
  Control Module/Device
- Check 2 errors are indicated by:
  Lighting Check 2 lamp on CE Panel. 3
  Stopping CU clock, if in error stop mode. 4
  CH branch decode 11 (Check 2) to microprogram. 2
- Microprogram collects Check 2 error indications by:
  Special Op 13 (0D), gate control interface errors to ND register. 1
  Special Op 14 (0E), gate channel interface errors to NA register. 5
- See SENSE 15, Format 2, Bytes 11 and 20 for Check 2 posting of sense information.

HOW TO DISPLAY CHECK 2 ERRORS

(If IMPL lamp is on, Check 2 conditions will have to be scoped.)

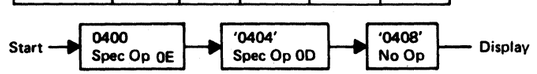
1. Set Operation Mode switch to Check Stop position.
2. Run machine until an error occurs. Check 2 and Clock Stop lamps on.
3. Do not reset error.
4. a. With SCU CE diagnostic disk in machine:
   (1) Set Operation Mode switch to Check Bypass.
   (2) Set IAR to '000C'.
   (3) Operate Start switch.
   (4) SB contains the (ND register) control interface error indications.
   SC contains the active CTL-I In Tags.
   SA contains the (NA register) channel interface error indications.

   b. With functional disk in machine:
   (1) Set Operation Mode switch to Check Bypass.
   (2) Ensure that TD register bit 1=0. (If not=0, manually set to 0.)
   (3) Set IAR to '06F8'.
   (4) Operate Single Instruction switch three times.
   (5) Display ND register for control interface error indications (see PANEL 15).
   (6) Display NA register for channel interface error indications.

ALTERNATE DISPLAY METHOD

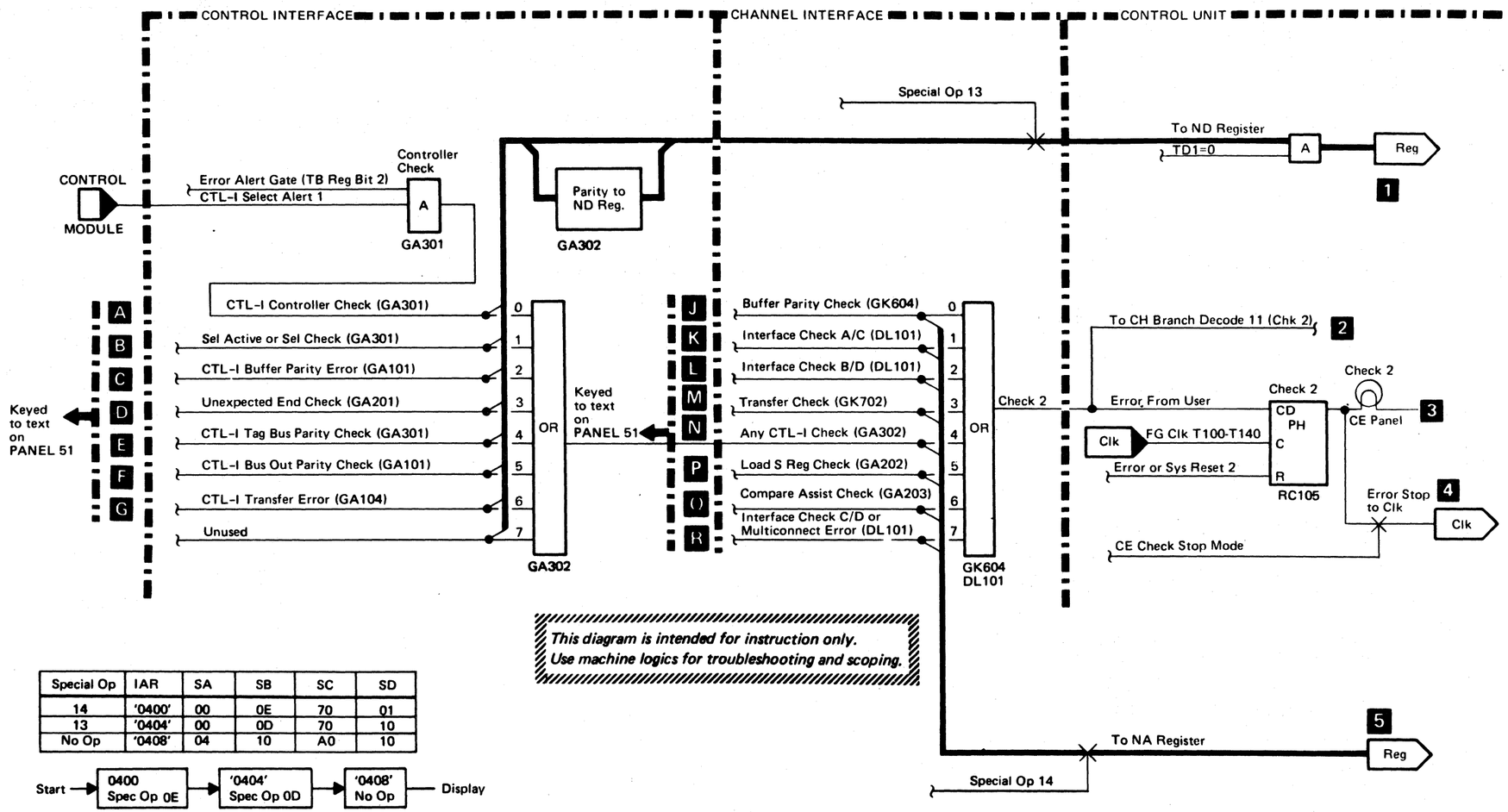
Enter the following display routine:

Special Op	IAR	SA	SB	SC	SD
14	'0400'	00	0E	70	01
13	'0404'	00	0D	70	10
No Op	'0408'	04	10	A0	10



Procedure for Loading Control Storage

1. '0400' to IAR.
2. Set up SA, SB, SC, SD (Spec Op 14).
3. Store.
4. Single instruction (will go to '0404' in IAR).
5. Set up SA, SB, SC, SD (Spec Op 13).
6. Store.
7. Single instruction (will go to '0408' in IAR).
8. Set up SA, SB, SC, SD (No Op).
9. Store.
10. Set IAR to '0400'.
11. Operate Single Instruction switch at least three times.
12. Errors will be stored in NA, ND registers.
13. Display NA, ND registers to determine Check 2 errors.



This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

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CHECK 2 ERROR COLLECTION (Part 2 of 2)

A CTL-I CONTROLLER CHECK (CTL-I 110)

If the controller detects an error during a control interface operation, it will raise Selected Alert 1. If Error Alert is active, Controller Check will be set. Error Alert (TB register bit 2) is kept active during most control interface operations.

B SELECT ACTIVE OR SELECT CHECK (CTL-I 115)

If device selection is lost (loss of either Select Active or Select Hold) during a control interface operation when Error Alert (TB register bit 2) is active, Select Check will be set. Error Alert is kept active during most control interface operations.

C CTL-I BUFFER PARITY ERROR (CTL-I 115)

Each time the CTL-I buffer is loaded, it is checked for correct parity. If parity is incorrect, correct parity is generated for the CU, and the Buffer Parity latch is set. Incorrect buffer parity is expected during some CTL-I operations (for example, polling sequences), and Buffer Parity Error is ignored by the microprogram at these times.

D UNEXPECTED END CHECK (CTL-I 115)

An Unexpected End Check occurs if the device attempts to end a data transfer operation prematurely. The check is set if Normal End is received during a Write operation, or if Normal End or Check End is received after the 1st Sync In pulse during a Read operation.

E CTL-I TAG BUS PARITY CHECK (CTL-I 115)

The CTL-I tag bus (TD register) is parity checked whenever Tag Gate is raised. If there is an even number of bits, Tag Bus Parity Check will be set.

F CTL-I BUS OUT PARITY CHECK (CTL-I 115)

If an even number of bits is detected in the CTL-I Bus Out selecter (bits 0-7 and P), the Bus Out Parity Check latch is set.

G CTL-I TRANSFER ERROR (CTL-I 120)

During a Read or Write operation, the transfer of data between the control unit and the control interface is monitored by the transfer check circuitry to ensure that the proper gating sequences have taken place.

In a Read operation, data is gated from CTL-I bus in to the CTL-I buffer and then to the MA register in the control unit. During a Write operation, data is gated from the TA register in the control unit to the CTL-I buffer and then to the CTL-I bus out.

A transfer error occurs if, while in a data response mode, a solid Sync In is received, or data is not properly transferred between two successive Sync In pulses. In a Read operation, the check is accomplished by verifying that the Sync In latch, the Buffer Full latch, the CH5 Branch latch, and the Gate External MA Register latch have set between two successive Sync In pulses. This same check is made in a Write operation except that the Gate TA Register to Buffer latch is checked instead of the Gate External MA Register latch.

J CHANNEL BUFFER PARITY CHECK (CHL-I 160)

Buffer parity check is set by even parity of data on Read and Write operations and when Address In or Status In is active.

K INTERFACE CHECK CHANNEL A (or C) (CHL-I 185)

L INTERFACE CHECK CHANNEL B (or D) (CHL-I 185)

These circuits check each channel interface for the following invalid conditions:

1. The CU is selected, and Selected Out is propagated.
2. Select Out is detected, the CU is not selected, and Select Out is not propagated.
3. Address In or Operational In, and Service In or Data In are active at the same time.
4. Operational In or Status In, and Service In or Data In are active at the same time.
5. Data Out and Command Out are active at the same time.
6. Command Out and Service Out are active at the same time.

If the Two Channel Switch, Additional, feature is installed, these error indicators are shared by the four interfaces. If an error occurs in interface C or D, the Interface Check C/D line (R) will also be set.

M CHANNEL TRANSFER CHECK (CHL-I 165)

Invalid sequence of channel transfer control latches.

N ANY CTL-I CHECK

Any of the CTL-I errors (A through G) brings up CTL-I Check. The microprogram checks this bit before reading CTL-I errors to ND register.

P LOAD S REGISTER CHECK (CTL-I 120)

This error is set if two S registers are selected at one time during a Load S Register operation.

Q COMPARE ASSIST CHECK (CTL-I 120)

During each compare cycle, the logic checks that the D Bus Zero and Carry latches are set properly. It does this by comparing the state of the latches with the ALU outputs (D Bus=0 and Carry) that set them. If either comparison is unequal, the compare check circuit is activated.

R INTERFACE CHECK C/D OR MULTICONNECT ERROR (CHL-I 185)

This error indication is provided with the Two Channel Switch, Additional, feature. If this line is active in the presence of an interface check (K or L), it means that the error occurred in interface C or D. If this line is active when there is no interface check (K or L), it means that more than one channel is selected, or no channel is selected.

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REGISTER DISPLAY CIRCUITS

SPECIAL REGISTER DISPLAY

Using instructions on PANEL 15:

1. Select a CE mode.
2. Select desired register (Check 1, IAR, BAR, DAR, or ACR).

Note: These registers have more than nine bits and are displayed in the Address/Check/Program Display lamps. Example given is to display the Check 1 register contents.

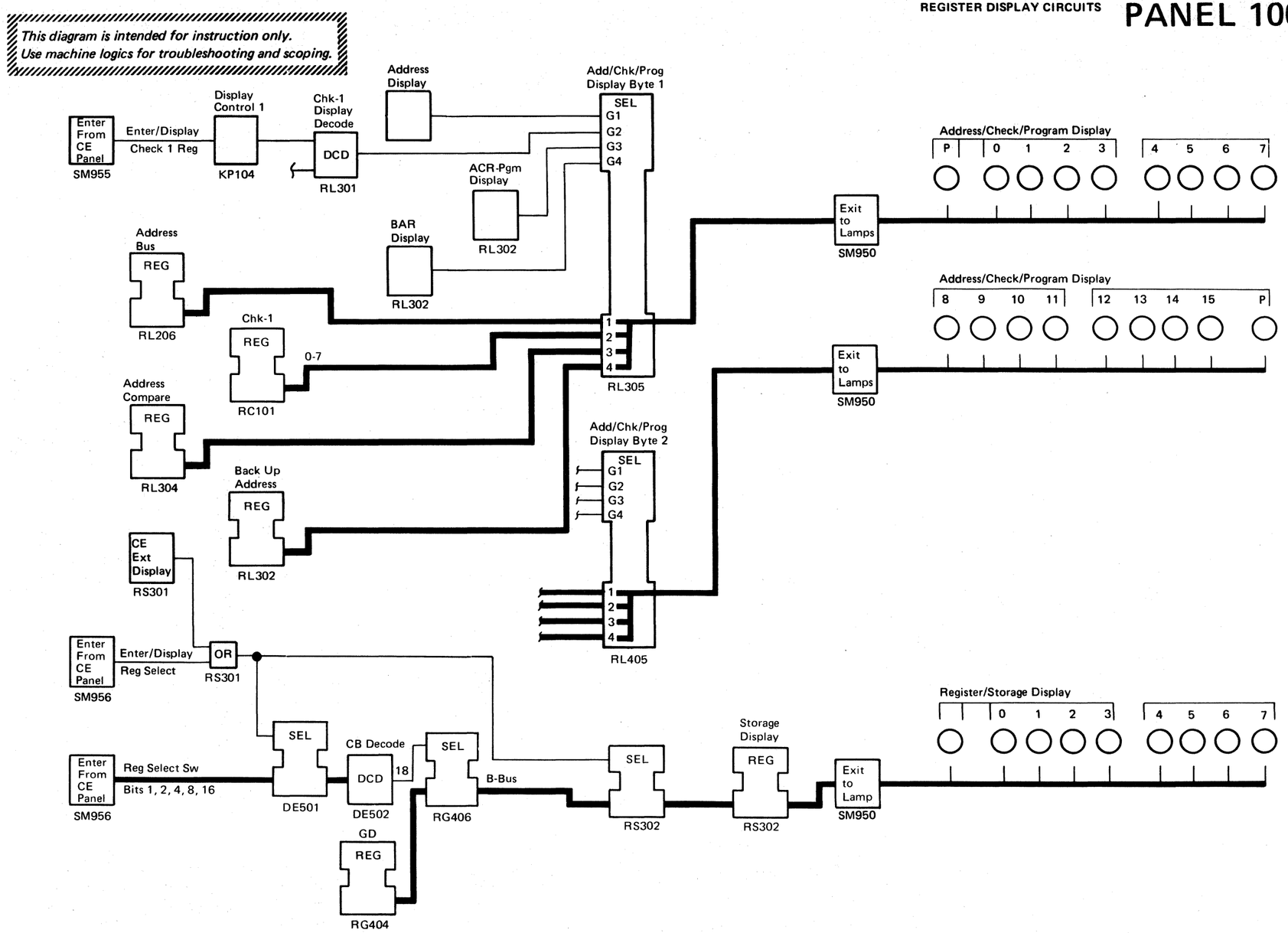
In any mode other than Normal, the two bytes of the Check 1 (or any other) special register may be displayed in the Address/Check/Program Display lamps. Byte 1 is stored in the Check 1 register and is gated to the Address/Check/Program Display lamps, positions 0-7, by the Enter/Display switch being in the Check 1 Reg position.

Byte 2 is entered into the Address/Check/Program Display lamps, positions 8-15, in the same manner as byte 1.

GENERAL PURPOSE REGISTER DISPLAY

1. Select a CE mode.
2. Set Enter/Display switch to Register Select.
3. Set Register Display switch to desired register. This conditions the CE Reg Select Bits 1, 2, 4, 8 lines. Bit 16 is set by the Inner/Outer switch in the Inner position.

The Register Select position of the Enter/Display switch gates the Reg Sel bits to the CB Decode. The CB Decode output selects a given register (in this case a decode of 18 selects the GD register) and gates that register onto the B bus. The B bus is gated by the Register Select line prior to entering the storage display register and the indicator lamps.



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REGISTER ALTER CIRCUITS (Part 1 of 2)

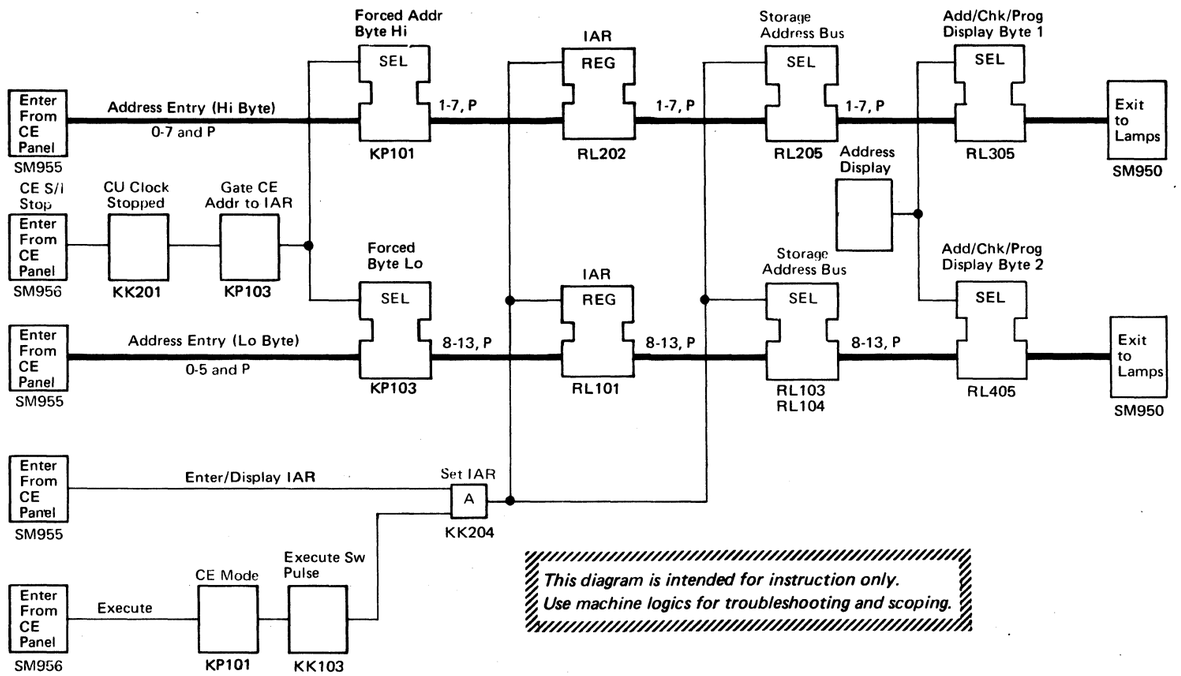
IAR REGISTER

The IAR register alter circuit is shown. The ACR register alter circuit is similar.

Stop the machine to bring up CU Clock Stopped. This gates the two bytes of data set in the Data Entry switches.

IAR Enter/Display switch line is ANDed with CE Mode when the Execute switch is operated, and this acts as the set for the IAR register.

Data is then moved through the storage address bus into the Addr/Chk Prog Display lamps for checking.



This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

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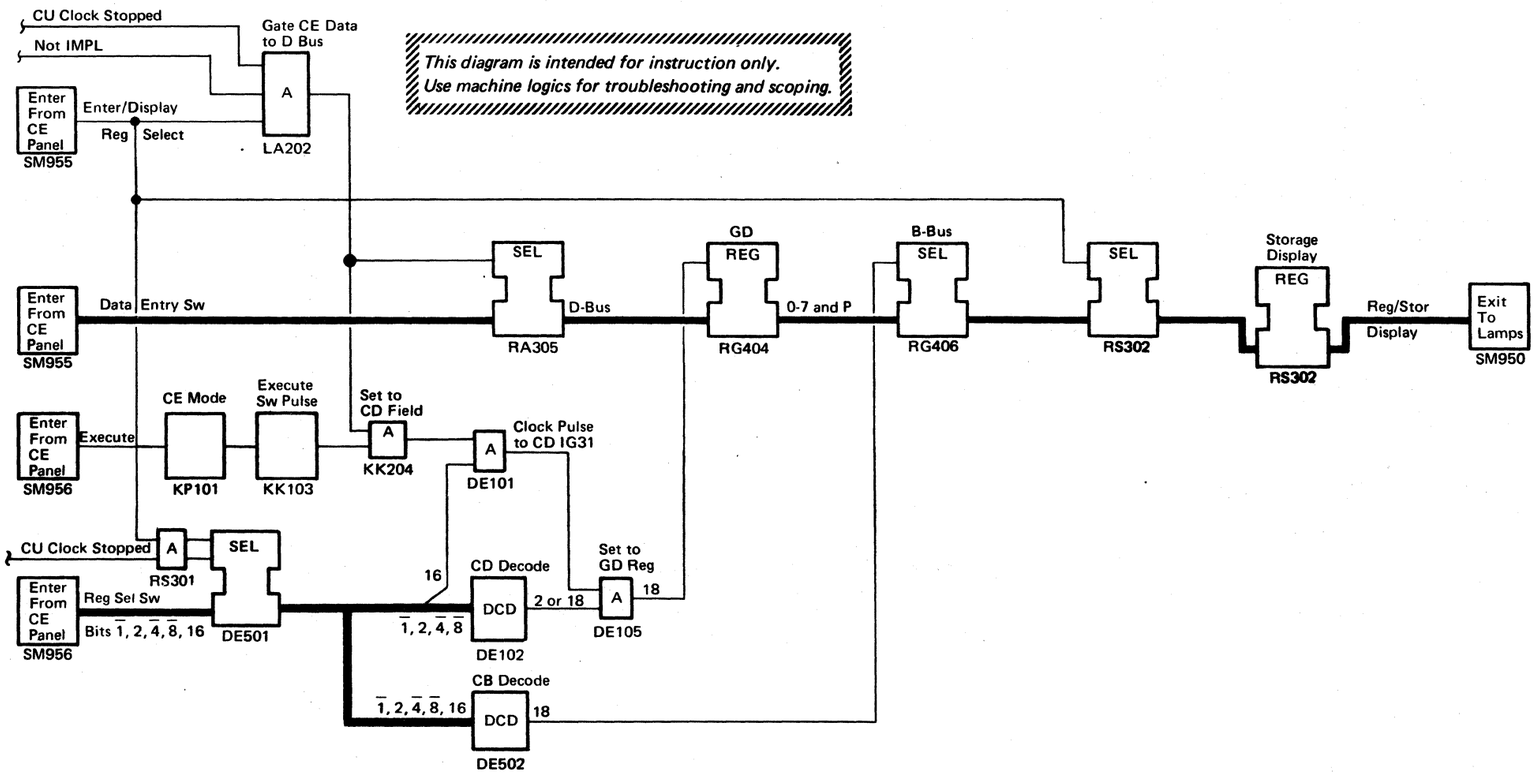
REGISTER ALTER CIRCUITS (Part 2 of 2)

GENERAL PURPOSE REGISTER

Clock Stopped and Not IMPL are ANDed to gate the CE Enter/Display Register Select signal. This signal is used to select the D bus as a path for the Data Entry switches from the CE panel. The Execute switch pulse is used to gate the bits generated by the Register Select switch.

Note: The register select switch consists of four binary sections (wafers) — 1, 2, 4, and 8 — which encode the register select bus using the same address scheme as the microcode fields CB and CD. (See MIC 3.) Bit 16 is encoded by the Inner/Outer switch being in the Inner position.

In this example the GD register is selected by a bit combination of 18 (bits 16 and 2). This decode of 18 serves as a gate to the GD register and also to the B bus assembler for displaying the GD register in the Register/Storage Display lamps.



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STORAGE ALTER AND DISPLAY CIRCUITS

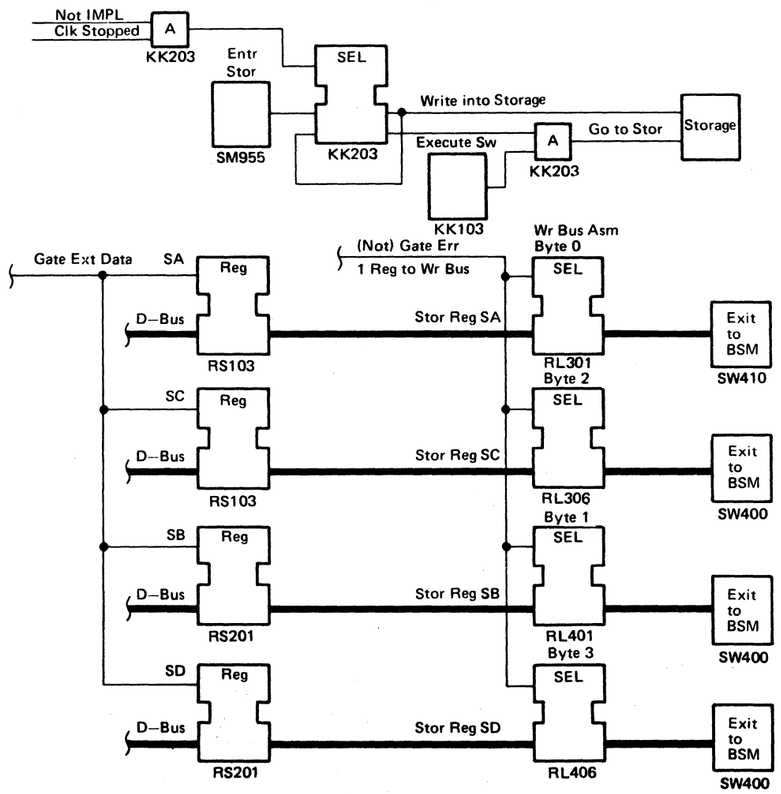
This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.

STORAGE ALTER

Load SA, SB, SC, and SD registers in the same manner as a general purpose register is loaded (PANEL 110).

Load IAR with the desired control storage address (PANEL 105).

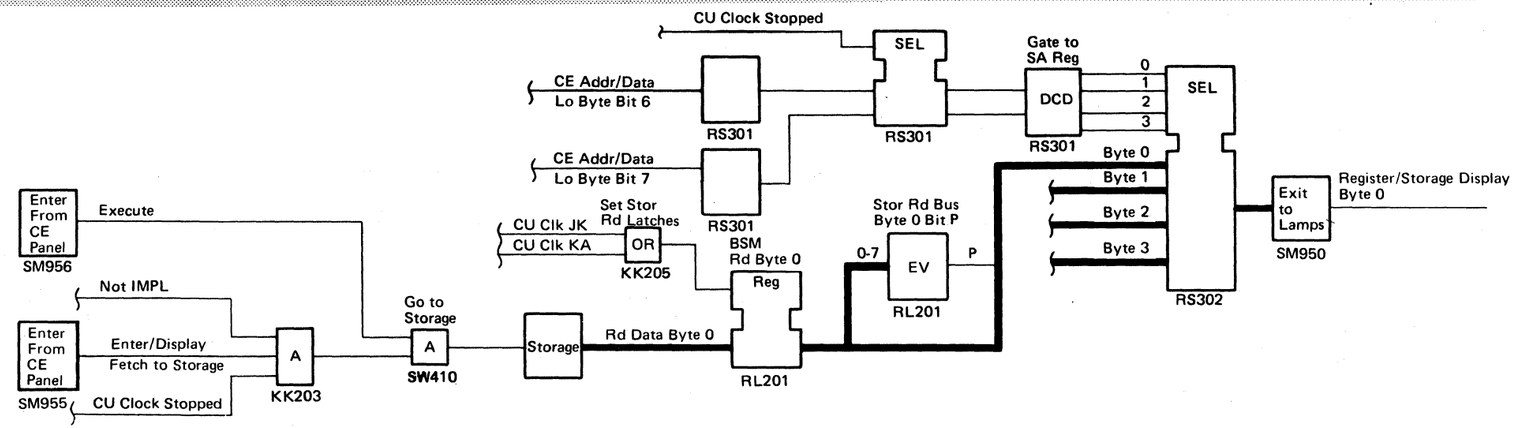
Select Enter Storage position of the Enter/Display switch and operate Execute to force a storage cycle and load the SA, SB, SC, and SD registers into the desired location.



STORAGE DISPLAY

Load procedure for setting the storage location in the IAR register is shown on PANEL 105.

Select Display Storage on the Enter/Display switch. This brings up the Enter/Display Fetch to Storage line. Operate the Execute switch to bring up the Go To Storage line in memory and make the data available on the storage read bus. The control storage bytes are gated by the Set Storage Read Latches. These are activated by CU Clock JK and KA pulses, which are active when the clock is stopped. Any of the four control storage bytes may be displayed by using the low order Data Entry Switch positions 0, 1, 2, and 3.



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ADDRESS COMPARE

ACR SYNC, STOP, OR RECYCLE

Select ACR to condition the address compare register (PANEL 16).

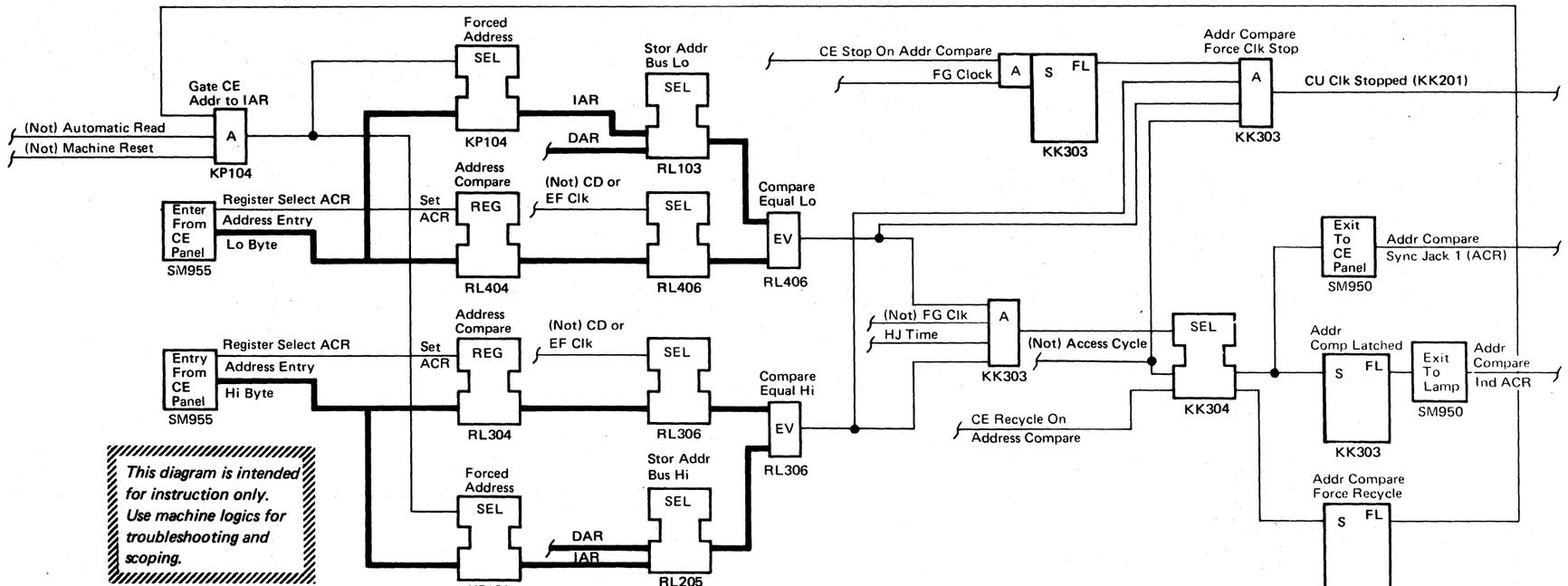
Set the Address/Data Entry switches to the address to be compared. Then operate the Execute switch to gate the address into the address compare register. At "(Not) CD or EF" clock time, the address is gated to the compare equal circuits. Here the instruction address is compared to the next address, which is the output of the storage address bus.

If the ACR switch is in the Sync position at HJ clock time after an equal compare, provided the CU is not in an access cycle, a 40-ns pulse will be available at the Address Compare Sync jack 1 (ACR) and the Address Compare indicator (ACR) will turn on. (See Note 1.)

If the ACR switch is in the Stop position at FG clock time after an equal compare, and the CU is not in an access cycle, the CU Clock Stopped line will become active and the machine will stop prior to executing the entered instruction address. The machine must be in a CE mode to be stopped.

If the ACR switch is in the Recycle position, a starting address can be entered to allow the machine to loop between two addresses.

At HJ time, after a Compare Equal, the Recycle position will turn on the Address Compare Force Recycle latch, which gates the starting address from the Address/Data Entry switches onto the storage address bus.

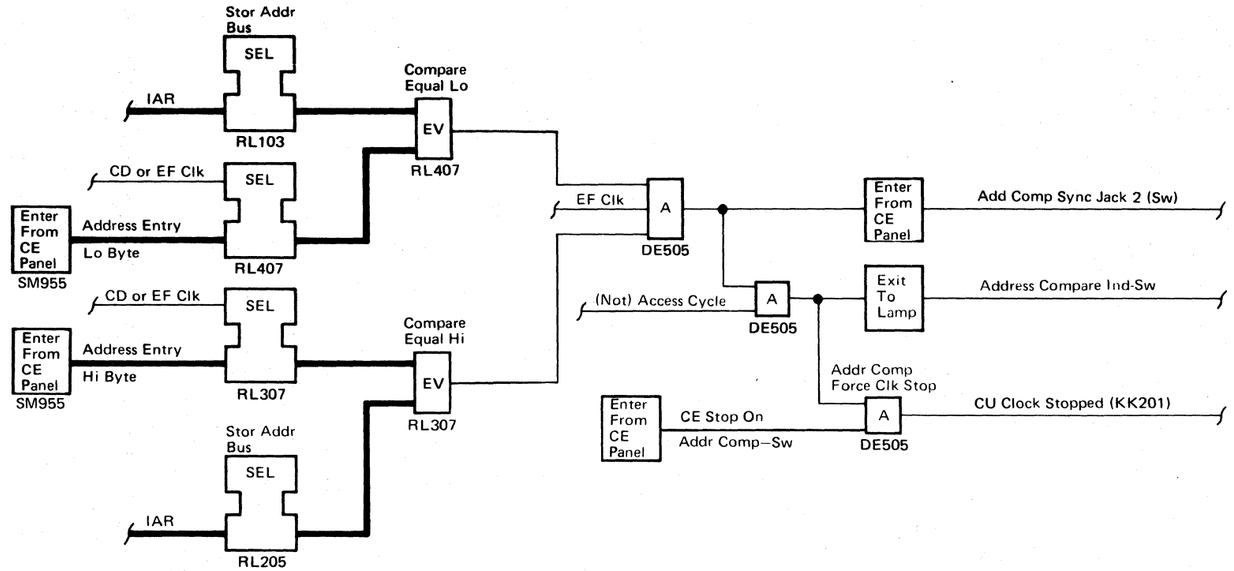


SW SYNC, OR STOP

With the switch in the Sync position,the address in the Address Entry switches is entered directly into the compare equal circuits at CD or EF clock time. There, it is compared against the storage address bus. When a Compare Equal occurs, a 40-ns pulse will be available at the Address Compare Sync jack 2 (SW) at EF clock time. (See Note 1.) If the CU is not in an access cycle, the Address Compare indicator – SW will be active.

In the Stop position, the stop signal from the CE panel is ANDed with the Address Compare Indicator signal at the address compare force clock stop block to activate the Control Unit Clock Stopped line to stop the machine. The machine cannot be stopped unless the CU is in one of the three CE modes.

Note 1: As an aid to troubleshooting in the device, sync pulses can be transmitted through the control interface cable to the device via the CE Communication Out driver. See CTL-I 10 for procedure.



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MICRODIAGNOSTIC ROUTINES SUMMARY

- Some routines or parts of routines may be looped; however, when they are restarted, they must be started with the first routine of the group.
- Many routines are divided into several tests, each of which may be individually looped. Such routines should be broken only between tests if at all possible.
- Some routines perform extensive checking of parameters entered by the CE. Since parameters must be entered before the routine is executed, they need be checked only once. Such a routine may then be divided into two sections: one to check parameters, and one to perform the actual test. Only the second section is then required in any scope loop.
- Hardcore routines are automatically executed during IMPL and cannot be run under control of the diagnostic monitor.
- Microdiagnostic messages are given in the Address/Check/Program Display lights. Refer to MICRO 25.

MICRODIAGNOSTIC ROUTINE ID

The following is a list, by routine ID, of the 3830-2 routines. Some routines are linked to run sequentially and are so indicated.

Routine ID	Name	Linked To	Routine Description	Operating Instructions	Error Code Dictionary
	HARDCORE				
HC00	Loader Setup Test	01	MICRO 60	START 25	Stop Words:
HC01	CA, CB, and CD Decode Test	02		START 25	MICRO 65
HC02	Loader Completion Test	03		START 25	Loop Words:
HC03	ALU Operations Test	04		START 25	MICRO 70
HC04	ALU Operations Test	05		START 25	Check 1's:
HC05	Register-To-Register Transfer Test	06		START 25	MICRO 150
HC06	ST Set/Reset, BR and ST Branch Tests	07		START 25	
HC07	Complete Disk Loader	08		START 25	
HC08	Storage Scan	09		START 25	
HC09	All Register Bit Set/Reset Test	0A		START 25	
HC0A	CI Static Test	0B		START 25	
HC0B	Channel Static Test	0C		START 25	
HC0C	Special Operations Test	End		START 25	
	CHANNEL WRAPAROUND				
60	System Reset	62	MICRO 210	MICRO 200	MICRO 215
62	Active Bus In, Bus Out, Tags, Branch Conditions	64	*(Also see*	MICRO 200	MICRO 225
64	Request In, Bus Out-Bus In Data Path	66	*MICFL*	MICRO 200	MICRO 255
66	Initial Selection, Halt I/O	68	*Section)*	MICRO 200	MICRO 270
68	Invalid Selection	6A		MICRO 200	MICRO 300
6A	Short Busy Sequence, Two Channel Switch	6C		MICRO 200	MICRO 305
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6E	Disconnect In, Selective Reset	End		MICRO 212	MICRO 340
	CONTROL UNIT				
86	ALU Branch Test	96	MICRO 400	MICRO 15, 400	MICRO 425
96	F Register Control	82	MICRO 403	MICRO 403	MICRO 440
82	Register Test	88		MICRO 15, 400	MICRO 405
88	Control Storage Test	84	MICRO 402	MICRO 15, 403	MICRO 430
84	Special Operations and Checkers Test	End	MICRO 400	MICRO 410	MICRO 410
8A	CE Panel Test	Independent	MICRO 402	MICRO 427	
	CONTROL INTERFACE				
8C	MC6, MC7, Load S Register	8E	MICRO 510	MICRO 500	MICRO 515
8E	Compare Assist, Tags	90		MICRO 500	MICRO 515
90	Recycle, Select Check, CL15	92		MICRO 500	MICRO 515
92	ST4, Buffer, Bus Out/In	94		MICRO 500	MICRO 515
94	Tags, Index, Response	End		MICRO 500	MICRO 515
0E00	Snipe Memory Stress Test	Independent	FSI 32B	FSI 32B	FSI 32B

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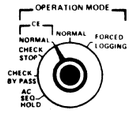
MICRODIAGNOSTIC LOADING PROCEDURE (Part 1 of 2)

CAUTION
Control unit microdiagnostics cannot be run inline with the customer program.

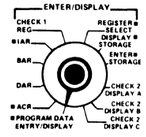
Note: Procedure A on START 25 must have been completed successfully before attempting the following procedure.

1 a. Vary offline all devices attached to this CU.
b. Turn off power on all control modules on the control interface.
c. Ensure that the Channel Enable/Disable switch(es) are in the Disable position.

2 Set Operation Mode to CE Normal.

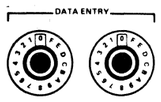


3 Set Enter/Display to Program Data Entry/Display.



See "Enter/Display Switch" on MICRO 20.

4 Set Data Entry switches to desired routine number.

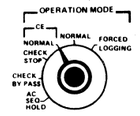


The maintenance routines are numbered '60' through 'FC'. Refer to MICRO 10 for index of routine descriptions.

5 Operate Execute switch.

The maintenance routine designated by the Data Entry switches is read from the MPL file and loaded into control storage locations '0400–05FC. While the routine is loading, message 1 is displayed in the program display indicators. (See MICRO 16 for message descriptions.) After a successful load, message 2 is displayed in the program display indicators. If the load is unsuccessful, message 3 or 4 is displayed. If the clock stops, go to FSI 30.

6 Set Operation Mode for hardware error control

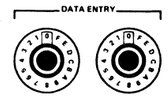


Selectable CE modes:

Selected Mode	Check 1 Error	Check 2 Errors
CE Normal	Machine stops	Ignored
CE Check Stop	Machine stops	Machine stops
CE Check Bypass	Ignored	Ignored
Forced Logging	Microprogram/ hardware selective reset	Ignored

CE Normal is recommended unless specified otherwise by an isolation procedure or by routine operating procedures (such as routine '60-6E', '84')

7 Set Data Entry switches for desired microprogram control option.



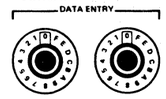
Loop options are '02', '04', '32'. Error control options are '3A', '01', '3E'. (See MICRO 16 for option descriptions.) If no error control option is selected, halt - on - error, '3E', will be in effect. The error control options ('3A', '01', '3E') are mutually exclusive; that is, only one option may be used at a time. However, the error control option may be changed while the routine is executing.

Note: Although an error control option can be entered, the option may not apply to a particular routine. (See control options on MICRO 210, 400, 510.)

8 Operate Execute switch.

Message 2 (MICRO 16) display continues. However, bits 2 and 3 of the display will indicate the error control entered. Refer to message 6 on MICRO 16 for definition of bits 2 and 3.

9 Set Data Entry switches for desired parameter control

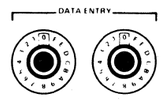


If default parameters are desired, enter '38'. (See MICRO 16 for control option descriptions). Then, proceed to step 12. To allow entry of parameters, place '10' in the Data Entry switches and proceed to step 10.

10 Operates Execute switch.

Message 5 will be displayed.

11 Set Data Entry switches for desired parameters.



Refer to MICRO 210, 400, 510 and enter the desired parameters. Repeat steps 10 and 11 until all parameters bytes are entered. Bits 4–7 of message 5 display will step with each parameter byte.

12 Operate Execute switch.

Diagnostic execution will begin as soon as defaults are accepted or the last parameter byte is accepted.

Message 6 will be displayed during execution of the routine.

Message 7 will be displayed after normal completion.

Message 8 will be displayed for program detectable errors. Refer to MICRO 25 for error display procedure.

Control option '00' (halt or resume execution) may be entered at any time.

For more detailed operating procedures, refer to the description provided in this section for each individual routine.

13 Terminate test. (See MICRO 20)

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MICRODIAGNOSTIC LOADING PROCEDURE (Part 2 of 2)

Messages

Address/Check/Program Display	Description
1 0 7 8 15 1000 0000 | Rtn No	The routine specified in the Data Entry switches is now loading from MPL file.
2 1100 0000 | Rtn No	The routine specified in the Data Entry switches is successfully loaded.
3 1000 1000 | xx00 000x	During loading of a routine, an error occurred. Attempt to reload. If error persists, analyze bits 8 through 15 and take action listed: Bit 8 MPL file read check - Go to MPL 15. Bit 9 MPL file seek check - Go to MPL 45. Bit 15 MPL file not ready - Go to MPL 30.
4 1000 1000 | 0010 0000	MPL file routine ID read compare error. Selected routine not on disk. This message is displayed if any disk other than CU diagnostic disk is inserted in 23FD.
5 11xx xxxx | Rtn No	Manual entry of parameters is required. Bits 4 through 7 define which parameter the routine requires. Fifteen entries are possible.
6 10xx 1111 | Rtn No Note: If check-1 indicators are on, refer to routine documentation for expected error. If check-1 not expected, go to FSI 30-55 for analysis.	The routine is now being executed, and no errors have occurred. Bits 2 and 3 identify the error control. '00' = Halt when an error occurs. '01' = Loop on first error. '10' = Continue on error.
7 11xx 0100 | Rtn No	Execution of the routine is halted because of one of the following: 1. Normal execution (without error) is completed. 2. Execution halted manually by data entry '00' command. 3. Display of error messages is complete (or was bypassed by CE). Bits 2 and 3 identify the error control. (See bit explanation under message 6.)
8 1000 0001 | Error Code	An error has been detected by the routine. Bits 8 through 15 define the error code. If more than one error byte is desired, enter '20' in the Data Entry switches and operate Execute. Up to 15 bytes can be displayed by repeatedly operating Execute switch. (See MICRO 25 for error byte display procedure.) Bits 4 through 7 indicate the error byte number. (Bypass remainder of display by '00' data entry.)

Control Options

Data Entry	Description
00	Halt or resume routine execution: Used for the following purposes: 1. Stop the routine. 2. Restart the routine after being halted for error display, or after being halted on error or normal end. 3. Bypass error display message active.
01	Continue routine on error: The routine continues running when an error occurs. At the end of the routine, a successful message is indicated in the program display indicators (Bits 2 and 3 are set to '10'.)
02	Bypass loop count: Forces the routine to run indefinitely. The routine will run until an error occurs or until manual intervention ('00' option or another routine is loaded.)
04	Inhibit link: Causes normal linkage to be inhibited. Only the routine loaded in control storage is executed.
10	Accept parameters from CE: Options '02', '3A', '01', or '3E' (if used) must be entered before option '10'. After entering option '10', enter parameters. Routine starts immediately after all parameters are entered.
20	Accept error message: Used for error display. When the program has error information available, message no. 8 is displayed. If more than one byte of error information is provided, the '20' entry will cause each additional byte to be displayed. Bits 4-7 indicate the error byte displayed in bits 8-15.
32	Loop program: Forces indefinite looping of all routines linked to routine being loaded. See MICRO 17 for details of this option.
38	Accept default parameter input: The routine uses predefined parameters and starts immediately.
3A	Loop on first error: The routine loops indefinitely on the first error detected (Bits 2 and 3 are set to '01'.)
3C	Display statistical data: Certain microprograms collect statistical data. To display this information, one '3C' entry must be made to initiate the display (thus halting program execution). Entry '20' is used for subsequent bytes. Bits 4-7 indicate the byte that is being displayed in bits 8-15 (same display as message no. 8).
3E	Halt on error: The routine stops when an error occurs (Bits 2 and 3 are set to '00'.)

Documentation References

Routine Number	Operating Instructions	Routine Description	Error Code Dictionary
HC00	START 25	MICRO 60	MICRO 70-74
HC01	START 25	MICRO 60	MICRO 74
HC02	START 25	MICRO 60	MICRO 76-78
HC03	START 25	MICRO 60	MICRO 80
HC04	START 25	MICRO 60	MICRO 82-84
HC05	START 25	MICRO 60	MICRO 86
HC06	START 25	MICRO 60	MICRO 92-94
HC07	START 25	MICRO 60	MICRO 96
HC08	START 25	MICRO 60	MICRO 96
HC09	START 25	MICRO 60	MICRO 98
HC0A	START 25	MICRO 60	MICRO 100-104
HC0B	START 25	MICRO 60	MICRO 106-108
HC0C	START 25	MICRO 60	Check-1 Only
60	MICRO 200	MICRO 210	MICRO 215-220
62	MICRO 200	MICRO 210	MICRO 225-240
64	MICRO 200	MICRO 210	MICRO 255-265
66	MICRO 200	MICRO 210	MICRO 270-290
68	MICRO 200	MICRO 210	MICRO 300
6A	MICRO 200	MICRO 210	MICRO 305-310
6C	MICRO 200	MICRO 210	MICRO 320-330
6E	MICRO 200	MICRO 212	MICRO 340
82	MICRO 400	MICRO 400	MICRO 405-408
84	MICRO 400	MICRO 400	MICRO 410-420
86	MICRO 400	MICRO 400	MICRO 425
88	MICRO 403	MICRO 403	MICRO 430
8A	MICRO 427 & 428	MICRO 402	
96	MICRO 403	MICRO 403	MICRO 440
8C	MICRO 500	MICRO 510	MICRO 515-555
8E	MICRO 500	MICRO 510	MICRO 560-595
90	MICRO 500	MICRO 510	MICRO 600-620
92	MICRO 500	MICRO 510	MICRO 625-685
94	MICRO 500	MICRO 510	MICRO 690-720

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LOOP OPTION 32 DESCRIPTION

What is Loop Option 32?

Loop option 32 is a special form of diagnostic control used to isolate intermittent failures.

Why Not Use Normal Running Procedures for Intermittent Failures?

Each set of diagnostics is written in a building block fashion; each step is based on the assumption that all previous steps have been executed without error. If an intermittent error occurs near the end of a series of tests, the error could be missed completely or cause the test to stop with an error code, which is misleading.

How Does Loop Option 32 Solve These Problems?

Loop option 32 eliminates the possibility of missing an error by looping the requested series of tests indefinitely. (For example, if the control interface tests are selected, all tests 8C-94 will be run. When they are completed they will be started over at the beginning and run again. This will continue until stopped by the CE.)

Loop option 32 eliminates misleading error codes by recording the errors that have occurred but displaying only the earliest error found during the series of tests.

When an error occurs the error code will be displayed for the CE, and testing will continue. If another error occurs later in the series of tests than that which is displayed, it will be ignored. If another error occurs earlier in the series than the one displayed, the display will be changed to the new error code, the number of tests being run will be decreased, and testing will continue.

How Do I Start Loop Option 32?

When loading the desired microdiagnostic (see page MICRO 15) at step 7, enter loop option 32 in the Data Entry switches and operate Execute. Go directly to step 11 — do not select error control.

How Will I Know If The Test Has Started?

While the tests are searching for an error, the 23FD file will be active and the program display lamps will flash the following:

1000 0000 Routine No. — A routine is being loaded

1000 1111 Routine No. — A routine is running

What Happens When An Error Is Found?

When an error occurs, the 23FD will still be active since the test is searching for more errors; however, the program display lamps will cease flashing. The *complete* error code will be displayed in the lamps and can be used for direct entrance to the Error Code Dictionary (for example, a lamp display of 1000 1110 0011 0100 is error code '8E34' and can be found on MICRO 560). The display will not change again until an earlier error is found.

What Do I Do When The Test Has Found The Earliest Error?

Go directly to the Error Code Dictionary and replace the suggested cards for that error code or load the diagnostic that failed using normal loading procedures; then set up the scope loop suggested by the Error Code Dictionary.

What Do I Do If The Test Keeps Running Without Finding An Error?

1. Tap on suspected cards.
2. Move trileads and cables.
3. Vary voltages slightly.
4. Let test run for a period of time.
5. The problem could be in a different section of the CU; try another set of diagnostics.

Which Tests Can Be Run Using Loop Option 32?

Three groups of tests can be run using this option. Not all routines of these tests may be used. Refer to the table at right to identify routines that will be used. Observe run comments for each group. Default parameters must be used with loop option 32.

Lamp displays that might occur other than those mentioned:

Prog Display Lamps				Meaning	Ref
1000	1000	1000	0000	MPL File Read Check	MPL 15
1000	1000	0100	0000	MPL File Seek Check	MPL 45
1000	1000	0000	0001	MPL File Not Ready	MPL 30
1100	0100	Routine	Number	Execution has been halted by the CE	

Loop Option 32 Test Groups.

Tests	Routines (In running order)	Comments
Channel Wraparound	60 62 ↰ 64 ┐ 66 Loop 68 Option 32 6A ┐ 6C ┘ 6E	Routine 60 initializes certain operations and must be started exactly as stated on MICRO 200. Substitute the following for step 10 on MICRO 200: Turn multi-tag switch on. Set Data Entry switches to '32' and operate Execute switch.
Control Unit Function Tests	86 ↰ 96 ┐ 82 Loop 88 Option 32 84 ┘	Forced Logging mode must be used to run this group of tests. See MICRO 400 for run instructions. Set Data Entry switches to '32' and operate Execute switch prior to step 5 of Operating Instructions if loop option 32 is desired.
Control Interface	8C ↰ 8E ┐ 90 Loop 92 Option 32 94 ┘	Follow Running Instructions on MICRO 500. Substitute the following for step 7: Set Data Entry switches to '32' and operate Execute switch. Set Data Entry switches to '38' and operate Execute switch.

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MICRODIAGNOSTIC OPERATING INFORMATION

Organization

The Maintenance Microdiagnostic Programs are a group of routines operated under a common Control Program. The Control Program resides in control storage upon completion of IMPL using CU diagnostic disk. Microdiagnostic routines are loaded via MPL using the CE Microdiagnostic disk.

A microdiagnostic program may consist of a number of routines which are linked together (that is sequentially loaded and executed).

Each microdiagnostic routine is identified by a Routine ID byte. Available routines are listed in the Microdiagnostic Routine Summary (MICRO 10). The Summary also indicates which routines are linked together to form microdiagnostic programs.

Operating Modes

Standalone Mode (See MICRO 15) must be used for execution of any 3830-2 microdiagnostic.

Operation Mode Switch

For Standalone Mode operations, switch to the CE Normal position.

The CE Check Stop and CE Check Bypass positions are used only when specifically called for in the comments column of the Microdiagnostic Routine Summary. Many microdiagnostics force error conditions and will operate properly only with the switch in its expected position.

Enter/Display Switch

During microdiagnostic operation, the position of this switch may be changed for the purpose of noting the contents of various registers. If this is done, be certain to return the switch to the Program Data Entry/Display position immediately after the desired information has been obtained.

The microdiagnostics communicate with the CE by placing information in the Address Compare Register (ACR) which is in turn displayed in the Program Display lamps when the Enter/Display switch is in the Program Data Entry/Display position. If the microdiagnostic attempts to place information in the ACR when the switch is in any position other than Program Data Entry/Display, the contents of the ACR will not be changed; then, when the switch is returned to Program Data Entry/Display position, the Program Display lamps will not contain the most current information.

Control Options

Control Options are normally selected immediately after routine loading (before parameter entry). However, options may be changed at any time except during parameter entry.

Only those Control Options that are applicable to the routine being run should be selected. The Microdiagnostic Routine Summary lists applicable Control Options for each routine.

Control Options '02', '3A', and '01' are automatically non-selected during routine loading. Options '3A', '01', and '3E' are mutually exclusive. If none of these are selected, the Halt on Error option ('3E') will be in effect.

Parameter Entries

Parameter Entries are used to provide additional control information to microdiagnostic routines. The number of parameters required varies depending on the routine being run. The Microdiagnostic Routine Summary indicates the number of parameters required by each routine and describes the content of each byte.

Most microdiagnostic routines provide default parameters. To use default parameters, enter '38' in the Data Entry switches and operate the Execute switch. The routine will begin execution.

To select Parameters as described in the Microdiagnostic Routine Summary, enter '10' in the Data Entry switches and operate the Execute switch. Then enter parameters in the Data Entry switches, operating Execute switch after each entry. Bits 4-7 of the Program Display lamps will indicate which byte should be entered next. All parameters must be entered in the order listed. After the last byte has been entered, the routine will begin execution.

Dynamic Control Options

Control Options may be changed at any time during routine execution. Refer to Control Options section.

To halt a routine that is running or to resume execution of a routine that is halted, enter '00' in the Data Entry switches and operate the Execute switch.

To change parameter entries for a routine that is already in execution, first halt the routine. Enter '10' in the Data Entry switches and operate the Execute switch. Then enter parameters in the Data Entry switches, operating Execute switch after each entry. All parameters must be entered in the order listed in the Microdiagnostic Routine Summary. After the last parameter has been entered, the routine will resume execution.

To force the last Error Message Display to be repeated, first halt the routine, then enter '3C' in the Data Entry switches and operate the Execute switch.

Termination

Normal termination of a microdiagnostic routine or a series of linked routines is indicated by the pattern 1100 0100 appearing in bits 0-7 of the Program Display lamps.

Upon completion of microdiagnostic use, the following steps should be performed prior to returning the facility to the customer:

1. Return the Operation Mode switch to the Normal position.
2. Re-install the customer's 23FD disk and perform an IMPL operation. Check that the IMPL operation is completed.
3. Return the control unit Channel Interface switches to the Enable position.

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3830-2/ISC MICRODIAGNOSTIC RATE SELECTOR – Routine 9F

PURPOSE

Routine 9F provides a variable run rate for drive microdiagnostics during concurrent maintenance. A run rate may be selected that is most compatible with the customer needs. For example, if microdiagnostics cause system degradation to the degree of impacting customer operations, the microdiagnostic rate may be reduced to minimize degradation. However, if it is desired to reduce the drive down time, an increased microdiagnostic rate may be selected.

Caution must be exercised when selecting a faster rate. Unless an alternate path is available to the string of drives, a faster rate will probably impact customer operation.

Note: The rate selection has no affect on stand-alone run times.

THEORY

System utilization of the 3830 directly affects the run rate of microdiagnostics. Regardless of the rate selected, if the system has not attempted to select the 3830 while microdiagnostics are being run, the diagnostic monitor proceeds immediately into the next diagnostic routine. If however, the system attempts to select the 3830 while microdiagnostics are being run, the 3830 forces a specified amount of time for system utilization. This time is varied with the parameter entered for routine 9F.

OPERATION

The range of run rates are from approximately 15 minutes to more than 2 or 3 hours (depending on system utilization) to run linked series routines 81 through 95. The customer should be consulted before deciding to either increase or reduce the microdiagnostic rate. The customer should be made aware that a faster rate could degrade system performance (depending upon utilization) and reduce down time. Also a slower rate, while lessening the impact the microdiagnostics have on system performance, may increase the down time.

RATE VERIFICATION READ OUT

If routine 9F is loaded and started without entering parameters, the current rate remains unaltered and is displayed in the Lo byte on the 3333 or the Data display on the 3340-A2 or 3350-A2. Rate verification should be performed prior to execution of microdiagnostics.

RUN PROCEDURE

The procedure to load and run routine 9F is as follows:

1. With the functional microprogram disk* in the 23FD and using procedures outlined on MICRO 10, load routine 9F from the controller drive CE panel. (Routine 9F resides on the functional disk, not the microdiagnostic disk.)
2. When the routine is loaded (3333 Hi display = xx00 1010 or 3340/3350 Program Control display = 1100 1010) select parameter from Table 1 to be entered. To select the optimum rate for the customers application it is recommended that parameter 04 (faster) or 06 (slower) be entered initially and then progressively faster (03 - 00) or slower (07, 08) rates be entered until the desired rate is reached. When the optimum run time has been determined for the subsystem, record the parameter used on the label (P/N 2345990) on the controller CE panels and drive microdiagnostic disk. If invalid parameters are entered, the routine defaults to 05 (normal rate).
3. Enter parameters:

   Control Entry '10' Parameter entry required. See MICRO 10.
   Parameter 1 'CE' Key Parameter required for rate entry.
   Parameter 2 'xx' Select from Table 1.
   Control Entry '00' Execute routine.
4. Successful execution of routine 9F is indicated: 3333 Hi display = xx00 1111, or 3340/3350 Program Control display = 1100 1111. A 3333 Hi display of xx00 0000 or 3340/3350 Program Control display = 1100 0000 indicates an invalid parameter (verify functional disk is installed). After rate has been altered, it remains as set until IMPL or changed by rate selector. IMPL of functional code sets rate to standard default value (05).
5. Load the microdiagnostic disk in the 23FD and proceed with microdiagnostics.

*EC 437462 or later.

Table 1

Enter Parameter	
00, 01, 02, 03, 04	Increasingly faster microdiagnostic rates. See *Caution*. 00 is fastest rate and has greatest impact on system performance.
05	Default value set by IMPL of functional code.
06, 07, 08	Increasingly slower microdiagnostic rate. 08 is slowest rate and has least impact on system performance.

CAUTION
Caution should be exercised when using these parameters as degradation may be more than the customer operation allows unless an alternate path is available. Faster rates may impact customer operation. Customer concurrence must be obtained.

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PURPOSE

The Tracer Dumper Micro (TDM) is useful in problem definition and solving. This routine is intended for difficult problem definition where the system is available, as required, for dumping the trace information. The system may encounter unrecoverable channel errors when the trace information is dumped to the host system. TDM resides as micro routine 90 on the functional microprogram disk. Its execution modifies 3830-2/ISC control storage so that activity on both the channel and controller interfaces is traced. (System throughput is not affected.) TDM also permits the trace tables, registers, and working storage to be read from the 3830-2 control storage into main storage for printing. TDM has three functions; the channel interface tracer, the controller interface tracer, and the dumper.

If functional microcode P/N 4168811 is being used, refer to CAS microfiche, QA page, P/N 4168831 for description and operation. If functional microcode P/N 4168816 is being used, refer to CAS microfiche, QA page, P/N 4168836 for description and operation. If functional microcode other than P/Ns 4168811 or 4168816 is being used, continue below.

CHANNEL INTERFACE TRACER

The channel interface tracer stores a word in the channel trace table every time the storage control unit attempts to present status to the channel, except for zero initial status. The overlaying channel trace table is located in control storage addresses 0400-04FF. Each four byte entry contains:

Byte	Contents	Byte	Contents
1	Unit Status	4 (bits 0–1)	01 – Channel B
2	Channel Command		10 – Channel C
3	The ST Register		11 – Channel D
4 (bits 0–1)	00 – Channel A	4 (bits 3–4)	Controller Address
		4 (bits 5–7)	Device Address

For example, a SIO to address 269 on channel B with a CCW chain of Seek, Read Home Address, would generate the following three entries:

Unit Status	Channel Command	ST Register	Chl/Unit Address
08	07	45	49
04	07	11	49
0C	1A	44	49

The trace table overlays or wraps around from 04FC back to 0400 when full. Thus it is necessary to determine the last entry in the table when tracing terminates. To do this, subtract 4 from the pointer byte located at 06F4 and add to constant 0400. For example, if the pointer byte at 06F4 is C4, then the last entry is at 04C0.

CONTROLLER INTERFACE TRACER

The controller interface tracer stores a world in the controller trace table every time the storage control unit issues a tag to a controller or drive, except for the poll tag (82) in the idel wait loop. The overlaying controller trace table is located in control storage addresses 0500–05FF. Each four byte entry contains:

Byte	Contents
1	RR, a microprogram return address indicator. RR bits 6–7 Return Address 00 2A04 + RR byte value 01 24FF + RR byte value 10 5A02 + RR byte value
2	PP, a pointer used to correlate control-I trace to channel-I trace. This controller trace entry occurred following the channel trace entry at 03FC + PP byte value.
3	The TA Register, CTL-I Bus Out.
4	The TD Register, CTL-I Tag Bus.

For example, using disk P/N 2348787, the first three entries generated in the initial selection after a SIO to device 0 are:

RR	PP	TA Register/ CTL-I Bus Out	TD Register CTL-I Tag Bus
70	08	00	83
C8	08	01	84
11	08	00	06

The first entry indicates the following: The microprogram return address is 2A74; bit 6 and 7 are off, so '70' is added to 2A04 for a return address of 2A74 (2A04 + 70). PP byte = '08' indicates that this entry in the CTL-I trace table occurred after the CHLI trace entry at address 0404 (03FC + 08). TA register indicates '00' was on CTL-I Bus Out. TD register indicates '83' was on the CTL-I Tag Bus.

The trace table wraps around from 05FC to 0500. The pointer in byte 2 is used to correlate each entry in the controller trace table to corresponding entries in the channel trace table.

To Begin Tracing

1. With the functional microprogram disk in the 23FD and using procedures outlined on MLM MICRO 10, load routine 90 from the controller drive CE panel. (Routine 90 resides on the functional disk, not the microdiagnostic disk.)
2. When the routine is loaded (3333 Hi display = xx00 1010 or 3340 Program Control display = 1100 1010), enter the parameters:

   Control Entry '10' Parameter entry required. (MICRO 10)

   Parameter 1 'DA' A key to prevent accidental use.

   Parameter 2 'XX' Selects which devices will be traced. Entering a valid controller/device address causes that one device to be traced. On 16 drive addressing storage control units, bits 0–3 are zero, bit 4 is the controller address, and bits 5–7 are the drive address. On 32 drive addressing storage control units, bits 0–2 are zero, bits 3–4 are the controller address, and bits 5–7 are the drive address. For example, to trace activity on channel/device address 356 (16 drive addressing), enter a parameter of '06'. Entering a parameter of 'AA' causes all devices on the storage control unit to be traced. Any other parameter will cause no devices to be traced.

   Control Entry '00' Execute routine.

3. When the routine execution is complete, the 3333 Hi display or 3340 Program Control display indicates its status:

   3333 Hi Display

xx11 1111	Successful run, tracing is in effect.
xx11 0110	The Key parameter is invalid.
xx11 0011	23FD read check occurred.
xx11 0010	The 23FD is not ready.
xx11 0001	23FD seek check occurred.

   3340 Entry 00 Execute routine.

1111 1111	Successful run, tracing is in effect.
1111 0110	The Key parameter is invalid.
1111 0011	23FD read check occurred.
1111 0010	The 23FD is not ready. [
1111 0001	23FD seek check occurred.

4. After executing routine 90 (successful completion or 23FD error) all CE panels are in a disabled state and OLTs will not run. The only way to terminate tracing or re-enable the CE panels and diagnostic commands is to re-IMPL the functional microprogram disk.

TO DUMP TRACE TABLES AND WORK AREAS

Only after execution of TDM can the two trace tables, control storage work areas, and register contents be read into main storage for printing.

CAUTION

The procedure for dumping causes the SCU clock to stop; the systems ability to recover is unpredictable.

1. Use one of the following methods to put the storage control unit into dump mode:

   Method A (Dynamic): This method is useful for analyzing an error when a micro instruction (sync address) unique to the error is known. Mode Switch to CE Normal and stop clock. Load the address of the unique micro instruction into the ACR, dial the data switches to 3C3C, turn on recycle, start the clock and begin system operation. When the clock stops, the error has occurred; quickly switch to Normal Mode to allow a Disconnect-In sequence. This may prevent channel timeout. Again the clock stops (IAR=3C4C); CU Busy is presented to all subsequent SIOs. Mode Switch to CE Normal and operate Start to start the clock; the dynamic IAR display is 3C50. At this time the storage control unit is in dump mode.

   Method B (Manual): Switch to CE Normal Mode, stop the clock, set the IAR to 3C3C, operate start, operate check reset, operate start twice; dynamic IAR display is 3C50. The storage control unit is now in dump mode.

2. If the SCU receives a system or selective reset, the clock will stop. The dump data has been protected. Start the clock to reenter dump mode.
3. If OLT release 9.0 or later version is installed, go to OLT 40 to continue.
4. Use the following procedure to read the dump data into main storage for printing. Issue an 82 command with a data length of 1536 to any device on the storage control unit. This reads the dump data into storage as specified in the 82 CCW. For example, this may be done with FRIEND as follows:

```
DEV = 140 (valid address for this SCU)
ENTER CCW LIST IN ENGLISH
cmd 82
   DL = 1536
loopl
go
        LOOP IS FINISHED ON UNIT 140
```

The dumped data now in storage can be printed with FRIEND:

```
ccw
003600 82 003AB0  200  0600
dmp1536,003AB0,00e
```

The dumped data is in this sequence:

Number of Bytes	Control Storage Addresses	Contents
512	0200-03FF	Usage/error records
256	0400-04FF	CHL-I Trace
256	0500-05FF	CTL-I Trace
256	0600-06FF	Working Storage
256	0000...xx00...3F00	Zero Boundary words

Upon entering the dumper (3C3C) the contents of the storage control unit registers are saved in control storage as follows:

Address	Register	Address	Register	Address	Register
06E0	ND	06E9	TA	06F3	TG
06E1	NC	06EA	TD	3C00	SA
06E2	NB	06EB	MA	3C01	SB
06E3	TC	06EC	MD	3C02	SC
06E4	GB	06ED	GC	3C03	SD
06E5	GA	06EE	BR	3D00	GE
06E6	TB	06EF	MC	3D01	NE
06E7	NA	06F1	ST	3D02	TE
06E8	MB	06F2	GD	3D03	ME

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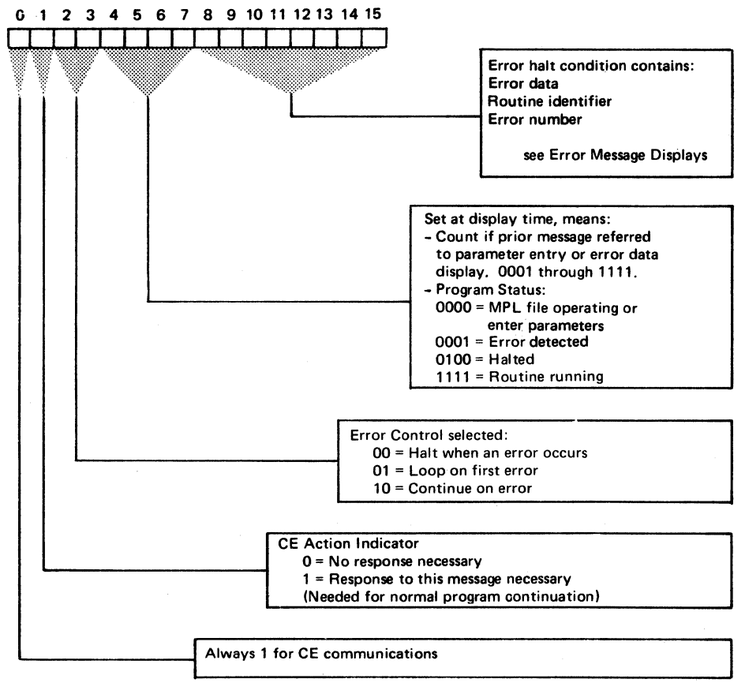
MICRODIAGNOSTIC OPERATION INFORMATION

CE LAMP DISPLAY

All microdiagnostic routine messages to the CE are displayed in the 16 Address/Check/Program Display lamps. The Enter/Display switch must be in the Program Data Entry/Display position for message display. See Loading Procedures on MICRO 15 and 16 for message descriptions.

MICRODIAGNOSTIC DISPLAY SUMMARY



ERROR MESSAGE DISPLAYS (CE lamp display)

An error message display may be recognized by the pattern 10XX 0001 appearing in bits 0-7 of the Program Display lamps. Bits 8-15 of the Program Display lamps contain the first message byte. Bits 4-7 indicate the message byte number.

Up to 15 message bytes may be available for display. The first message byte is the error number. When an error message display occurs, the following steps should be performed:

NOTE: Record all message bytes.

1 Error halt '81XX'

Record the hex value of bits 8-15. They will be used to form the error code.

2 Set '20' in the Data Entry switches and operate Execute switch to display next message byte. (The number of message bytes is variable)

3 After first Execute

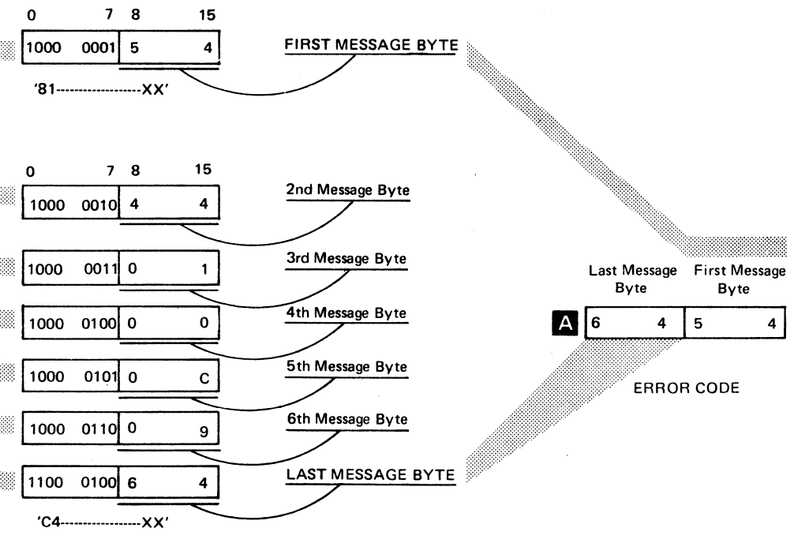
After second Execute

After third Execute

After fourth Execute

After fifth Execute

After sixth Execute



4 Observe that bit 1 = 1 now. Also bits 4-7 = 4 ('C4XX'). Now the message is complete.

The display will not change with more operations of Execute switch.

To repeat the display of the error messages from the error halt, set '3C' in the Data Entry switches and operate Execute switch; then return to step 2.

5 The last byte displayed is the routine number. Combine the last byte displayed with the first byte to form the error code. In the example, the error code equals 6454. A

6 Locate the error code in the Microdiagnostic Error Code Dictionary in the following MICRO pages to determine your next action.

ROUTINE	REFERENCE
60 – 6E	MICRO 215 – 345
82 – 86, 8A	MICRO 405 – 427
98	MICRO 430
9A	MICRO 440
8C – 94	MICRO 515 – 695

7 To continue routine execution enter '00' in the Data Entry switches and operate the Execute switch.

8 To terminate testing refer to MICRO 20.

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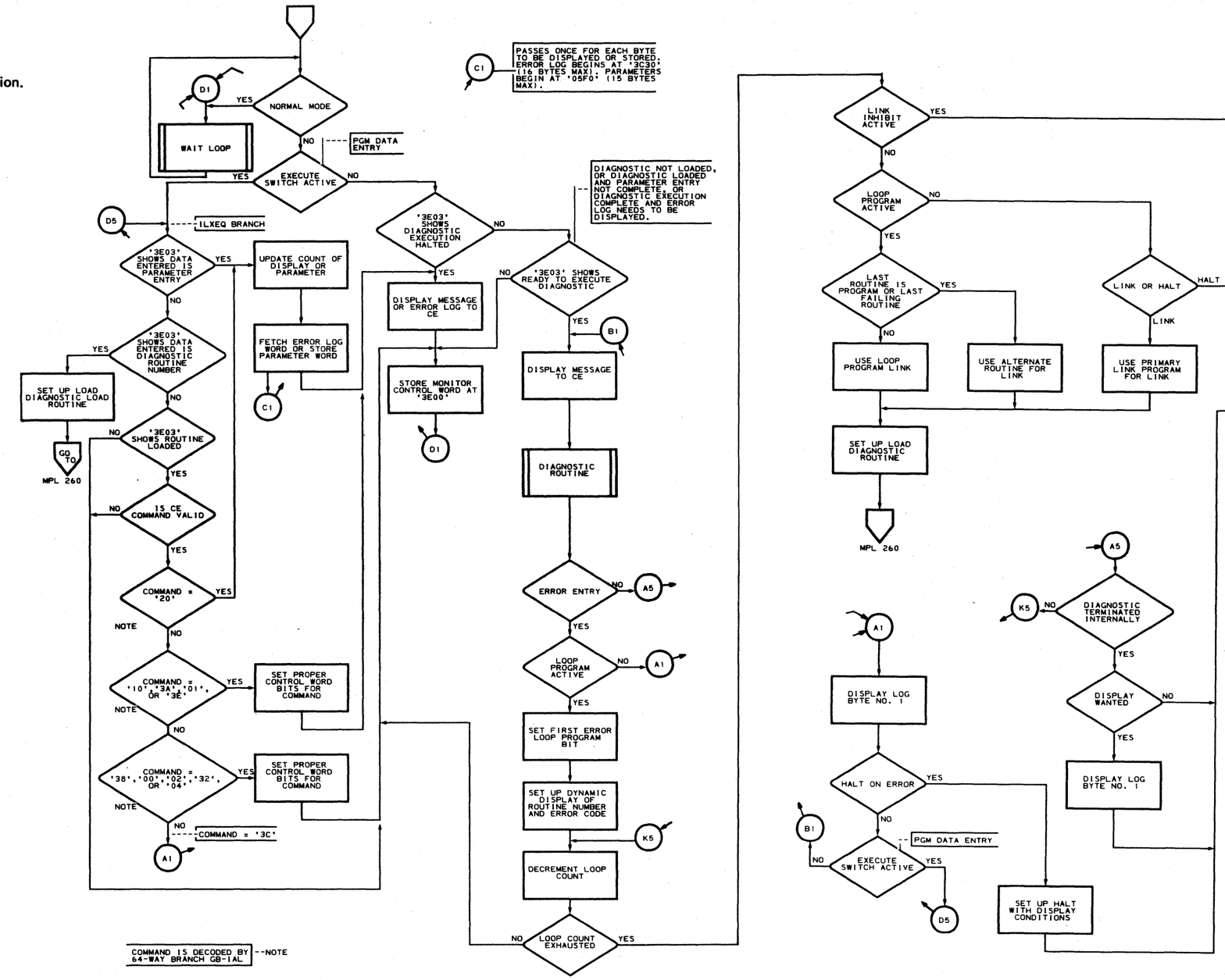
- Tests for CE inline and execute switches active.
- Exits to load diagnostic routine (MPL 260).
- Controls CE entry of parameters.
- Exits to execute the diagnostic routine.
- Controls display of error codes and error log information.
- Controls entry/re-entry/exit of diagnostic routine.



CONTROL WORD BREAKDOWN

'3E00' = DISPLAY CODE HI ORDER BYTE
'3E01' = DIAGNOSTIC ROUTINE ID
'3E02' = BIT 0 = DIAGNOSTIC BEING LINKED
'3E03' = BIT 0 = TURNED ON BY INITIAL PASS THRU DIAGNOSTIC CONTROL AFTER FORCED LOGGING SWITCH ACTIVATED
BIT 1 = DIAGNOSTIC IS LOADED
BIT 2 = DATA ENTRY IS ROUTINE NUMBER OR CE COMMAND
BIT 3 = PARAMETER ENTRIES ARE COMPLETE
BIT 4 = HALT EXECUTION OF DIAGNOSTIC ROUTINE
BIT 5 = DISPLAY CONNECTION (ON FOR ERROR LOG DISPLAY)
BIT 6 = NOT INITIAL ENTRY TO DIAGNOSTIC ROUTINE
BIT 7 = BYPASS LOOP COUNT

CE COMMAND SUMMARY

'38' = USE DEFAULT PARAMETERS
'20' = REQUEST NEXT ERROR BYTE DISPLAY
'00' = REVERSE STATUS (IF RUNNING, HALT. IF STOPPED, START. IF DISPLAYING ERRORS, BYPASS DISPLAY)
'02' = BYPASS LOOP COUNT
'3A' = LOOP ON ERROR
'01' = CONTINUE ON ERROR
'3E' = HALT ON ERROR
'10' = REQUEST PARAMETER ENTRY
'04' = INHIBIT LINKING
'3C' = DISPLAY STATISTICAL DATA (ERROR LOG)
'32' = LOOP PROGRAM (ALTERNATE LINK)

AU0500 Seq 2 of 2	2347003 Part Number	437402A 15 Mar 72	437403 21 Apr 72	437404 23 Jun 72	437405 15 Aug 72	437408 16 Oct 72	437414 4 Jun 73	

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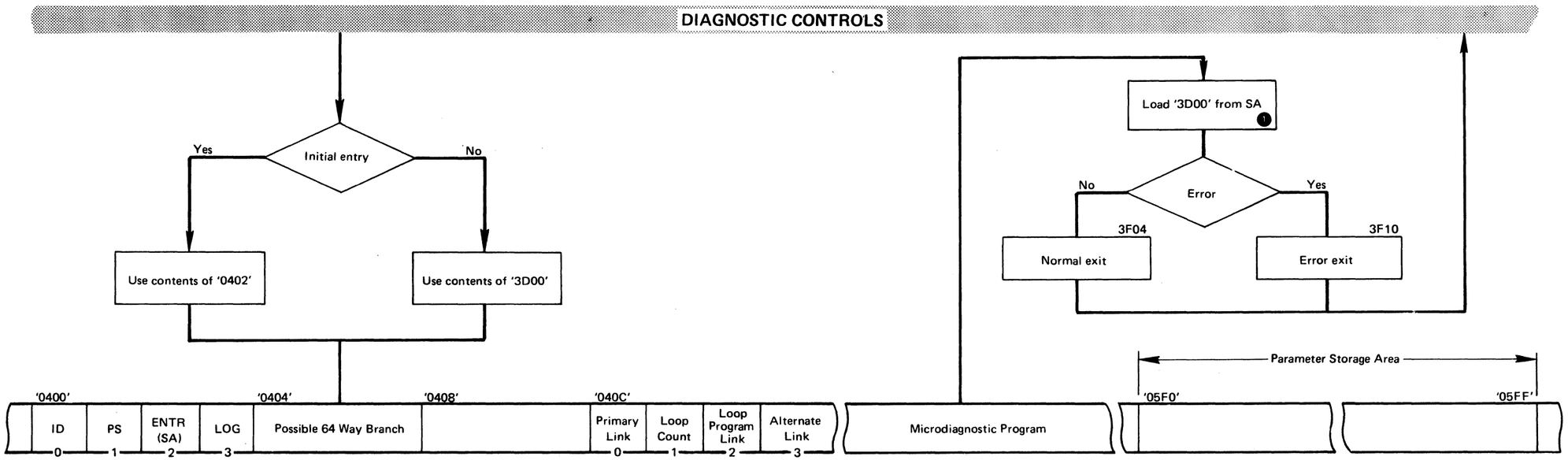

Byte 0 = ID = Routine ID (equal to high address byte of memory sector reflected in pseudo address and equal to even sector (of pair) address identifier).

Byte 1 = PS = Program Status Code for use by the control program.

Bit 0 = Parameters necessary (specified in documentation) and default parameters present.

Bit 1 = Do not pass parameters to this routine. (If bit 0, 1 = 1)

Bit 2 = Unused

Bit 3 = Pass only parameter byte 1 to this routine.

Bits 4, 5, 6, 7. = Binary representation of the number of parameters to enter.

For example: '0001' = 1 parameter entry
'0101' = 5 parameter entry
'1111' = 15 parameter entry (maximum)

Byte 2 = ENTR = Initial entry word specification. Will be gated into register SA for diagnostic use on initial entry only.

Byte 3 = Bits 0, 1, 2, 3. Unused

Bits 4, 5, 6, 7. = LOG = Binary representation of number of error data bytes that will be set up in diagnostic log area.

Byte 0 = Primary Link. If program completes execution successfully, the link provides next routine to be executed, except where inhibit link or loop program have been activated.

Byte 1 = Loop Count. Number of times routine execution repeated before terminating.

Byte 2 = Used as Primary Link when loop program command is initiated.

Byte 3 = Alternate Link. When loop program is activated and the Primary Link value is '00', the Alternate Link field provides next routine ID to be executed. If error exit occurs or has previously occurred, the Alternate Link field provides routine ID to be executed.

1 ADDRESS '3D00'

Byte 0 = Return byte set up by diagnostic to faciliate proper control return (if using 64-way branch at '0404'). Contents will be in SA register upon control return to the diagnostic.

Bytes 1, 2, 3. = Used by diagnostic to store any 3 registers upon control exit and restored by control to S registers before control return.

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HARDCORE TEST SUMMARY

The first hardcore test (HC00) is loaded from the 23FD disk by the hardware IMPL loader which loads track 0, sector 0, into control store locations '0000' through '00FF'. These first 64 words do simple tests in those areas required by the simple loader at the end of the test. The first few words check that certain address bits can be set/reset and that CA, CB, and CD decodes can be accomplished without error. When a *program* detected error occurs, the test goes into a one word loop, the address of which will be used in the MLM to locate the failing component. When a *hardware* detected error occurs, the clock stops with a check-1 light. BAR and check-1 register are used in the MLM to locate the failing component.

After the first test (HC00) is completed without error, the simple loader at the end starts loading track 0, sector 1, into control storage positions '0100' through '01FF'. This loader and the one used in HC01 do very little in the way of error checking. The only errors recognized are the BTRDY/SECTOR errors detected by the 23FD. The check sum is not tested for correct transfer of data until track 0, sector 3, (HC03) is loaded.

The second test (HC01) checks the CA, CB, and CD decodes of all standard registers not previously tested. The registers are not checked for correct data assimilation, but only test the decoder. If an error occurs, the BAR address and check-1 register contents indicate the type of error encountered and the SA register indicates which is the failing register decode.

When HC01 has been successfully executed, its loader reads from the 23FD and stores HC02 in control storage positions '0200' through '02FF' then branches to the first word in that test. HC02 is another of the hardcore tests, and completes testing enough hardware that its extended loader may be used. This is the last of the hardcore tests that checks only the loader requirements, then basic hardware testing begins.

The ALU operations not previously used are checked in HC03 and HC04. Data transfer to and from registers is checked in HC05. HC06 checks branch conditions in the BR and ST registers and tests the ability to set and reset the bits in the ST register (CS decode).

HC07 is the complete disk loader with extended error detection and track seek ability. It seeks to track 1 and loads and executes HC08. Quick storage scan is performed by HC08 which tests 0-4K of control storage except modules 00, 01, 07, and 08. The test writes all testable areas, then reads back each position and checks what has not been read.

The next test to be loaded and executed is HC09. This is the second register test and is designed to beat-pattern each register in turn and proceed to the next if the register operates correctly. The TC and TB registers required special handling and not nearly so extensive testing because of their ability to create check-2 errors and, thereby, abort the test. The GB register is treated as an exception because, during testing of the other registers, it is used as a pointer to designate which register is being used. HC0A and HC0B are, respectively, the CTL-I and channel static branch conditions tests. Then, HC0C executes each special op to test for check-1 condition on decode.

Upon successful operation of all the MPL tests '0F0F' is displayed in display lights. After proper CE response the remainder of control storage is loaded from the 23FD file and the diagnostic monitor idle loop is executed. Diagnostic routine 86 is loaded automatically and 'C086' is displayed awaiting CE response.

Control Storage Contents After Disk Loaded

Location	Contents
'0000'-'00FC'	System/Selective Reset
'0100'-'01FC'	23FD Disk Label
'0200'-'06FC'	'EF EF 55 55'
'0700'-'07FC'	Complete Disk Loader (HC07)
'0800'-'08FC'	Control Storage Addressing/Pattern
'0900'-'09FC'	Register 2 (HC09)
'0A00'-'0AFC'	CTL-I (HC0A)
'0B00'-'0BFC'	Channel (HC0B)
'0C00'-'3FFC'	Normal Load

Hardcore Test Identification

CS 0000 - Hardcore 0	(HC00)
CS 0100 - Hardcore 1	(HC01)
CS 0200 - Hardcore 2	(HC02)
CS 0300 - ALU 1	(HC03)
CS 0400 - ALU 2	(HC04)
CS 0500 - Register 1	(HC05)
CS 0600 - Stat Set/Reset, Branch Setting	(HC06)
CS 0700 - Complete Disk Loader	(HC07)
CS 0800 - Control Storage Addressing/Pattern	(HC08)
CS 0900 - Register 2	(HC09)
CS 0A00 - CTL-I	(HC0A)
CS 0B00 - Channel	(HC0B)

Load-and-Test Sequence of Events

1. Load '0000' to '00FC' and Execute HC00 — (IMPL) – Hardcore Test
2. Load '0100' to '01FC' and Execute HC01 — CA, CB, and CD Decodes
3. Load '0200' to '02FC' and Execute HC02 — Hardcore Test
4. Load '0300' to '03FC' and Execute HC03
5. Load '0400' to '04FC' and Execute HC04 — ALU
6. Load '0500' to '05FC' and Execute HC05 — Register 1 Test
7. Load '0600' to '06FC' and Execute HC06 — Status Set/Reset, Branching Test
8. Load '0700' to '07FC'

Note: Disk Loader now Residing in Control Store Module 7

9. Seek to Track 1
10. Load '0800' to '08FC', Display '0800', and Execute HC08 — Quick Scan

Note: Control Store Positions 0-4K Except Modules 0, 1, 7, and 8 Contain Last Data Pattern Written ('EF EF 55 55').

11. Load '0900' to '09FC' and Execute HC09 — Register 2 Test
12. Load '0A00' to '0AFC' and Execute HC0A — CI Static Test
13. Load '0B00' to '0BFC' and Execute HC0B — Channel Static Test
14. Load '0C00' to '0FFC', Execute HC0C, and Display '0F0F' — Special Ops Test
15. Seek to Track 2
16. Load '1000' to '17FC'
17. Seek to Track 3
18. Load '1800' to '1FFC'
19. Seek to Track 4
20. Load '2000' to '27FC'
21. Seek to Track 5
22. Load '2800' to '2FFC'
23. Seek to Track 6
24. Load '3000' to '37FC'
25. Seek to Track 7
26. Load '3800' to '3FFC'
27. Seek to Track 16
28. Load Sector 0 to Module 0 ('0000' - '00FF')
29. Load Sector 1 to Module 1 ('0100' - '01FF')
30. Branch to Idle Loop

Recycling On Undefined Errors

If an error occurs that is not in the Error Code Dictionary, A loop can be set up to recycle on the error stop word back to the beginning of the failing test:

1. Set error stop address in the ACR.
2. Set IAR to beginning address for that test as indicated in chart at right. (See PANEL 16 for instructions on Address Compare Recycle operation.)

H.C. Test	Address Begin	Address End
HC00	0000	00A0
HC01	0110	017C
HC02	02E4	02CC
HC03	03BC	039C
HC04	04C0	04B4
HC05	0560	0554
HC06	0600	06E4
HC08	0800	088C
HC09	0900	09B0
HC0A	0A00	0AD4
HC0B	0B00	0BEC
HC0C	0C00	0C30

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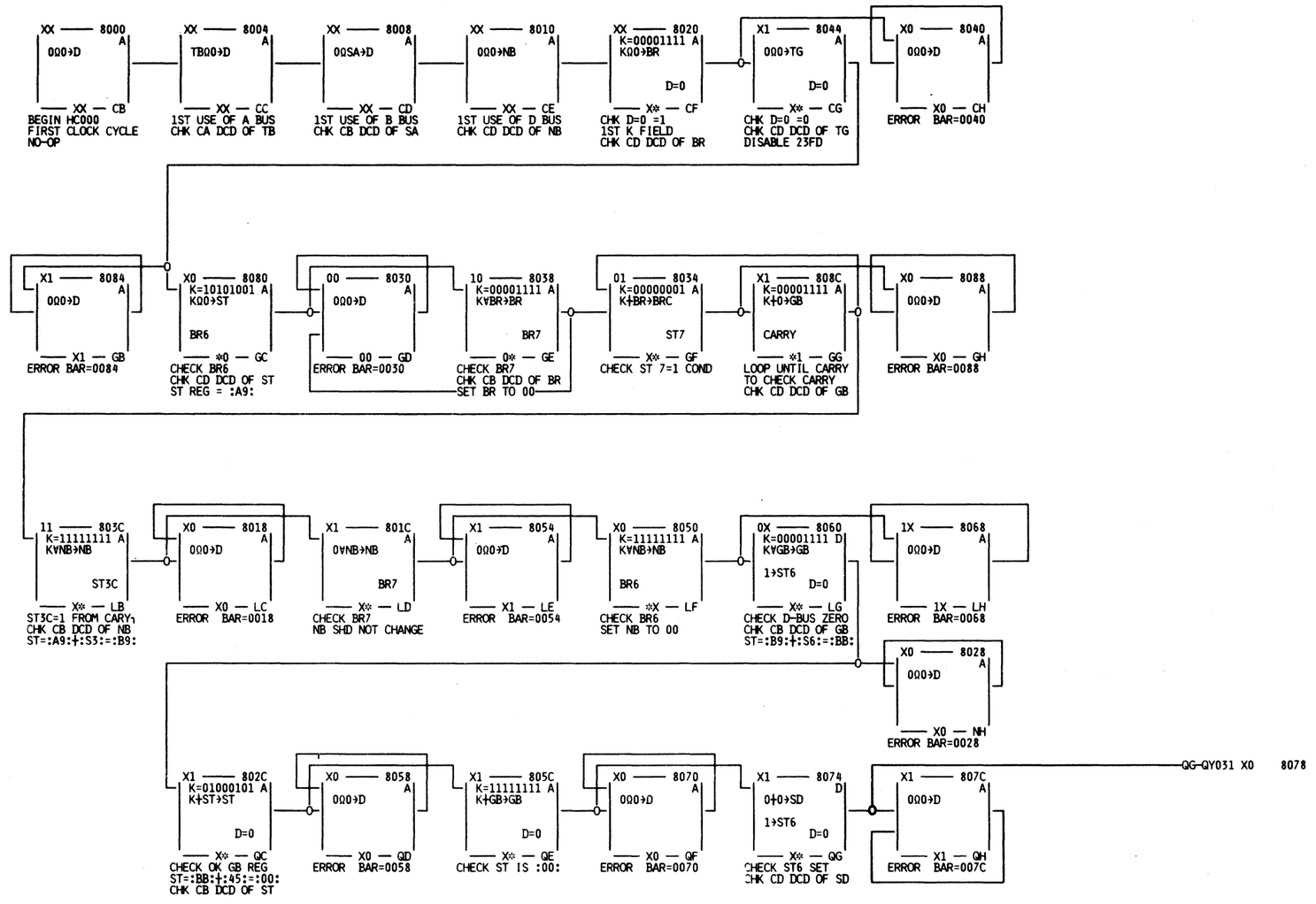
CAS (HARDCORE ROUTINE 00)



IBM CORP.	QY030 - HARD CORE - 00 (HC00)	MACH XXXXXXXX
PN		VER QY030
DATE 05/23/73		
LOG 13:05		

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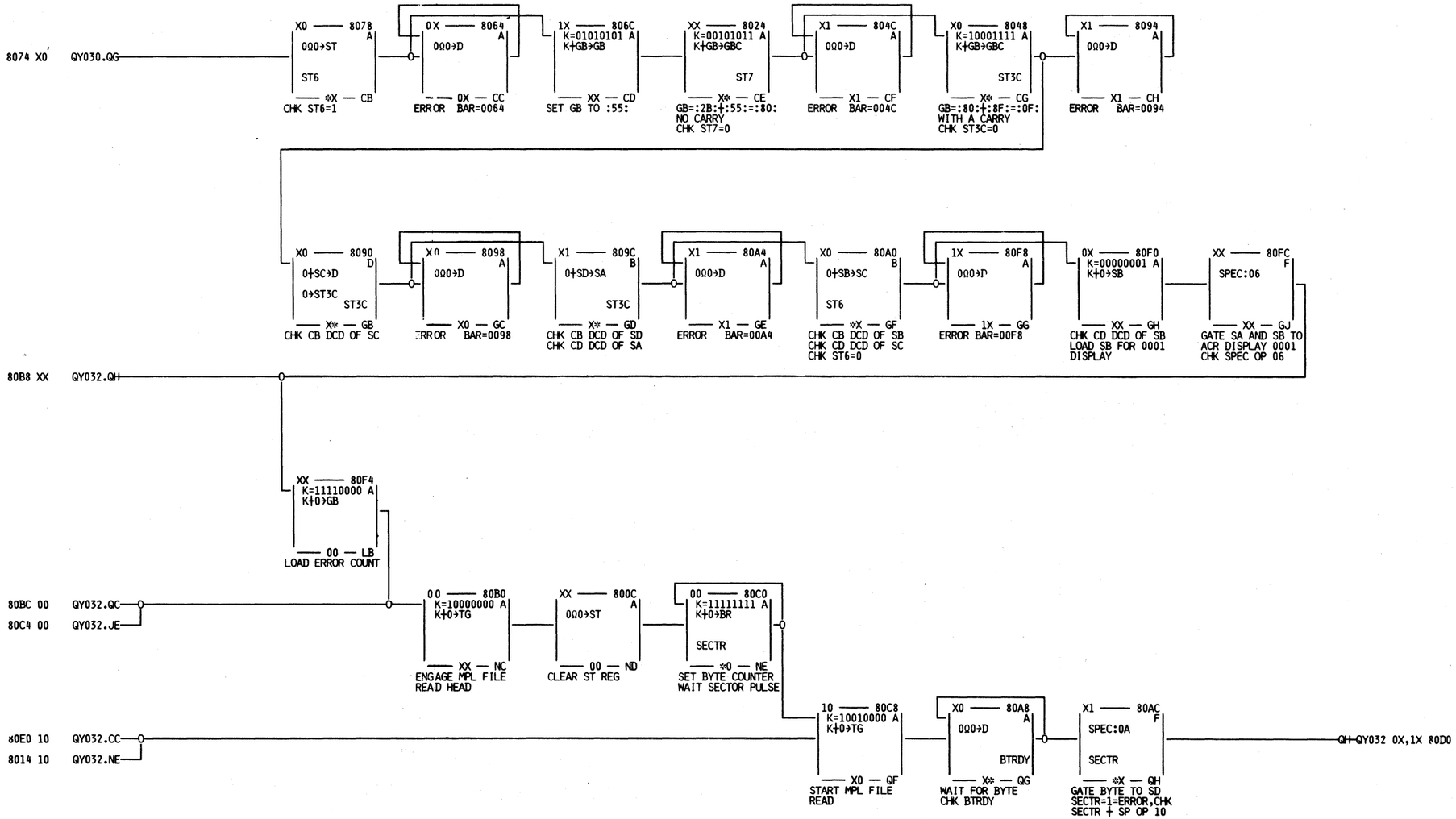
CAS (HARDCORE ROUTINE 00) **MICRO 62B**



QY031

IBM CORP.	QY031 - HARDCORE - 00 (HC00)	MACH XXXXXXXX
PN		VER QY031
DATE 05/23/73		
LOG 13:05		

AU0730	2354737
Seq. 2 of 2	Part No.( )

437414							
4 Jun 73							

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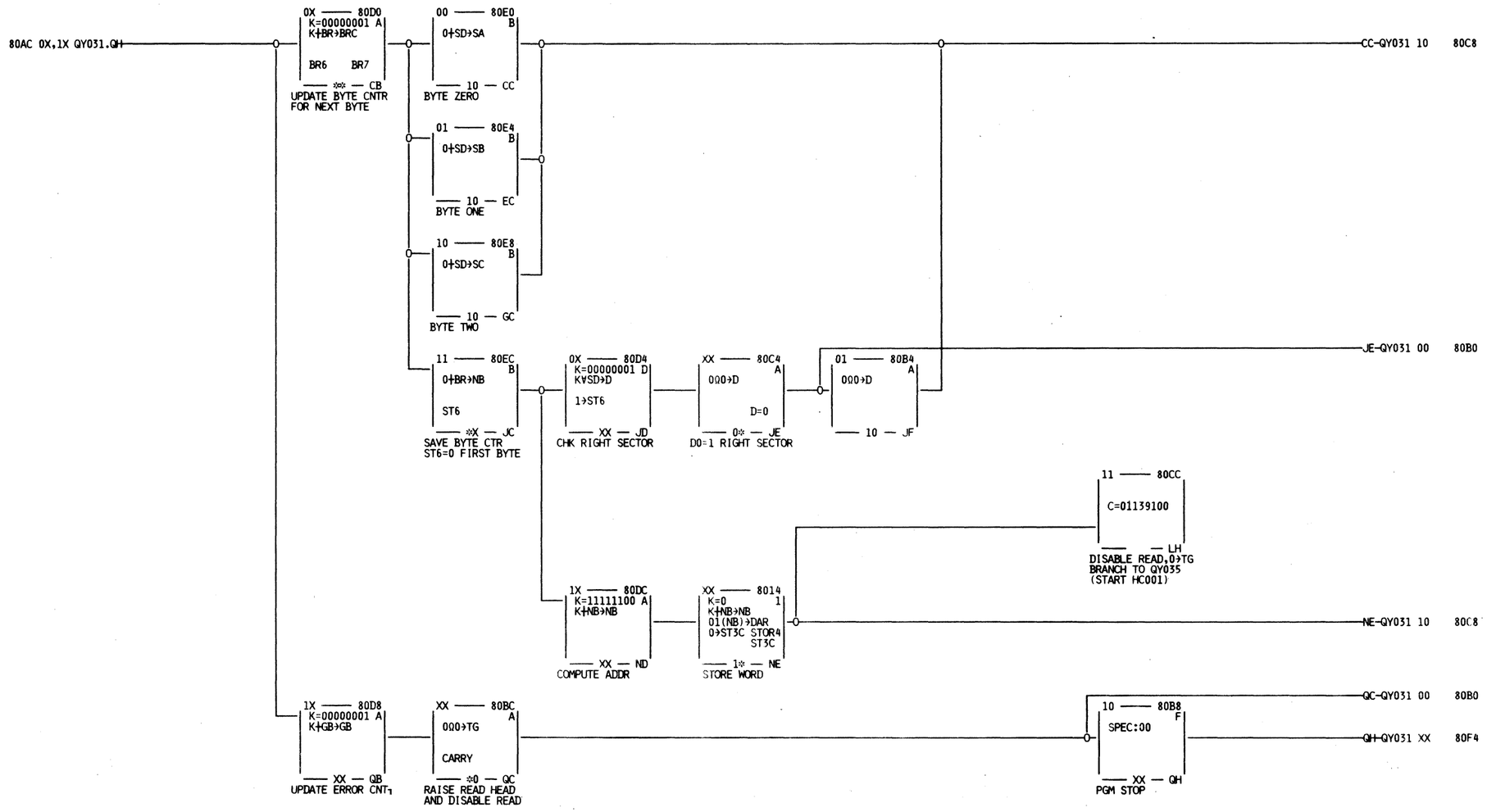
CAS (HARDCORE ROUTINE 00) MICRO 62B

CAS (HARDCORE ROUTINE 00)



QY032

IBM CORP.	QY032 - HARD CORE - 00 (HC00)	MACH XXXXXXXX
PN		VER QY032
DATE 05/23/73	LOADER	
LOG 13:05		

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CAS (HARDCORE ROUTINE 01) **MICRO 62D**

QY035

IBM CORP.			MACH XXXXXXXX
PN		QY035 - HARD CORE - 01 (HC01)	VER QY035
DATE	05/23/73	CB/CD DECODE	
LOG	13:05		

AU0740	2354738	437414						
Seq.2 of 2	Part No.( )	4 Jun 73						

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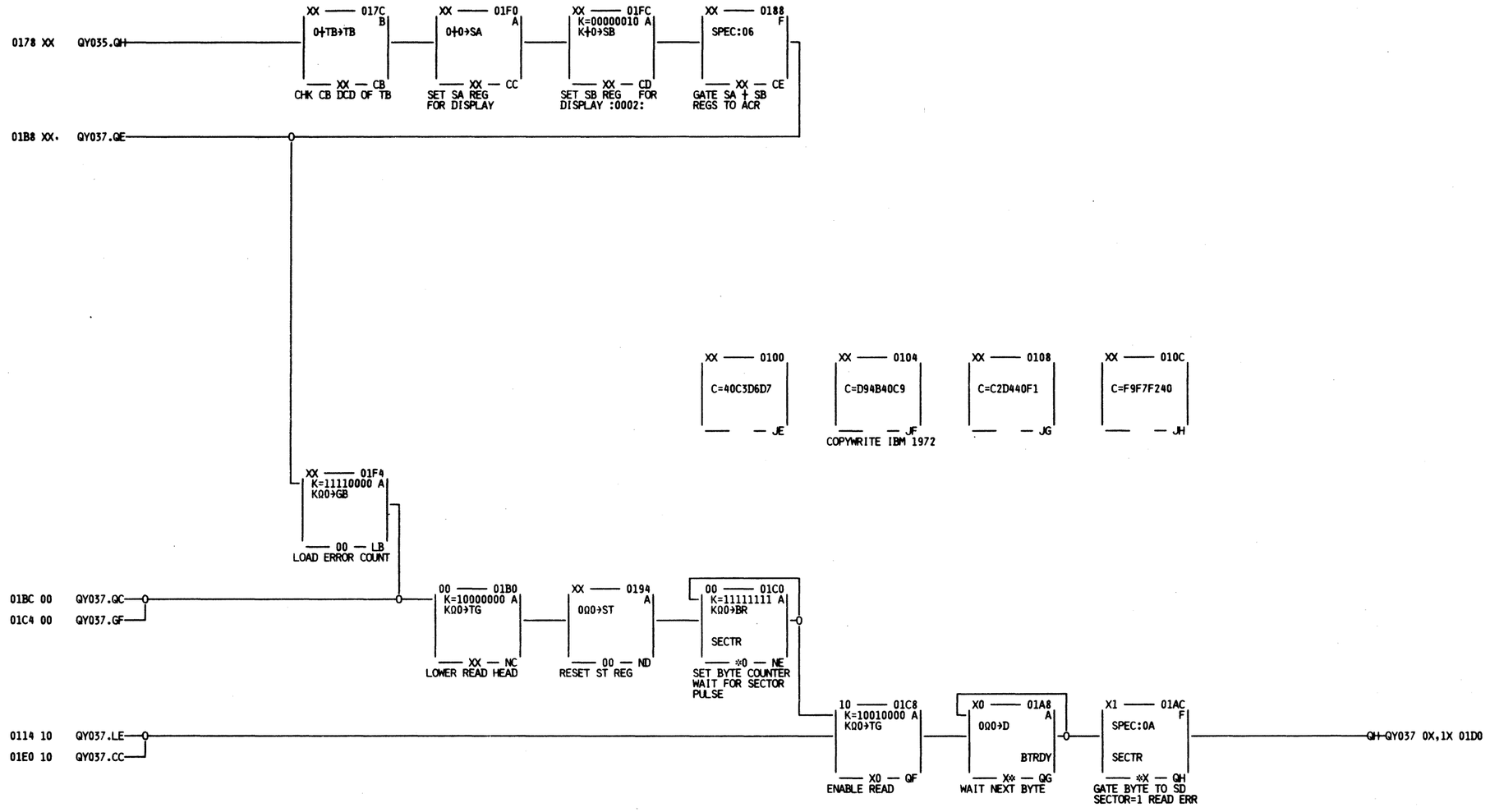
CAS (HARDCORE ROUTINE 01) MICRO 62D

CAS (HARDCORE ROUTINE 01) **MICRO 62E**



QY036

IBM CORP.			MACH XXXXXXXX
PN		QY036 - HARD CORE - 01 (HC01)	VER QY036
DATE	05/23/73	CA DECODE/LOADER	
LOG	13:05		

AU0750	2354739	437414						
Seq. 1 of 2	Part No.( )	4 Jun 73						

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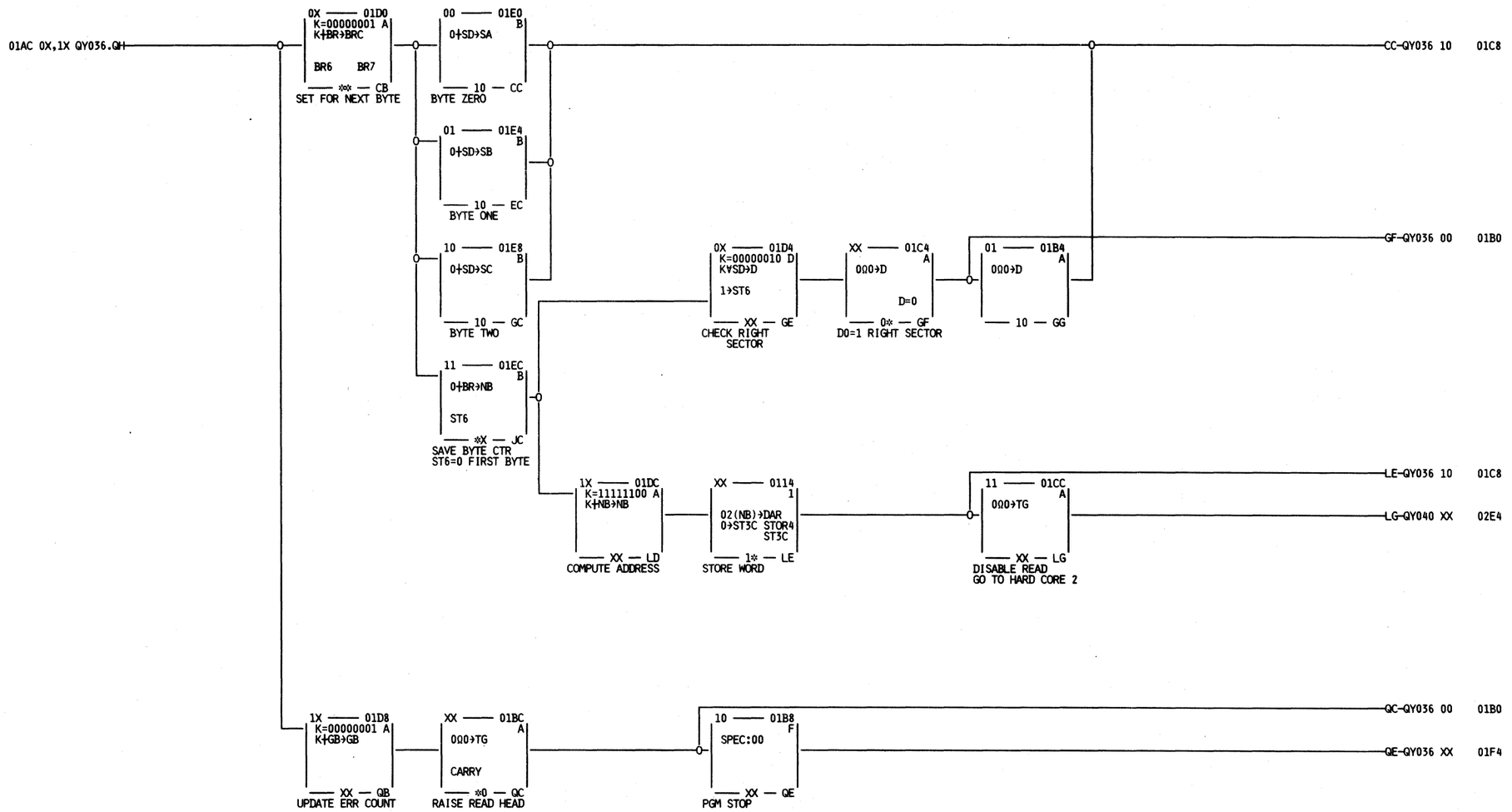

QY037

IBM CORP.			MACH XXXXXXXX
PN		QY037 - HARD CORE - 01 (HC01)	VER QY037
DATE	05/23/73	LOADER	
LOG	13:05		

AU0750	2354739	437414						
Seq. 2 of 2	Part No.( )	4 Jun 73						

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (Hardcore Routine)

STOP WORD LIST

1. Match BAR indication (hex) with listing on these pages until a match is found. Take action indicated.
2. Refer to START 900-909 for data flow by card and common card information.

<table>
<tr><th>BAR (hex)</th><th>Possible Failing Replaceable Units</th><th>Reference</th><th>Error Description and Comments</th><th>Recycle Addresses</th><th>CAS</th></tr>
<tr><td>0054</td><td></td><td></td><td>End of Check 2 display routine. Normal stop after setting IAR to '000C' and operating Start switch. SA, SB, and SC registers contain Check 2 conditions. See table:
<table>
<tr><th>Bit</th><th>SA Register (Check 2 Errors from NA Register)</th><th>SB Register (Check 2 Errors from ND Register)</th><th>SC Register (Active Inbound CTL-I Tags)</th></tr>
<tr><td>0</td><td>Buffer Parity Check</td><td>Controller Check</td><td>Selected Alert 1</td></tr>
<tr><td>1</td><td>Interface Check A/C</td><td>Select Active Check</td><td>Select Active</td></tr>
<tr><td>2</td><td>Interface Check B/D</td><td>CTL-I Buffer Parity Check</td><td>Sync In</td></tr>
<tr><td>3</td><td>Transfer Check</td><td>Unexpected End</td><td>Ignore</td></tr>
<tr><td>4</td><td>CTL-I Check</td><td>Tag Bus Parity Check</td><td>Normal End</td></tr>
<tr><td>5</td><td>Load S Register</td><td>CTL-I Bus Out Parity Check</td><td>Check End</td></tr>
<tr><td>6</td><td>Compare Assist</td><td>CTL-I Transfer Error</td><td>Tag Valid</td></tr>
<tr><td>7</td><td>Interface C/D or Multiconnect</td><td>Not Used</td><td>Not used</td></tr>
</table>
(See PANEL 50 for ECD of Check 2 error collection.)</td><td></td><td></td></tr>
<tr><td>00B8</td><td>B2S2, B1S2, B1T4, B2F2 B2L2</td><td></td><td>Threshold of 23FD error retry reached (normally 16 errors)
• If this is the only MPL disk failing with this symptom, try reseating the disk. If failure continues, suspect bad disk.
• If more than one MPL disk fails, go to MPL checkout on START 35, entry A.
• Check cables to and from MPL file. (Refer to logic page SS011.)
• Check MPL file adjustments per MPL section. Suspect motor speed, belt slippage.</td><td></td><td>See MICRO 62.</td></tr>
<tr><td>01B8</td><td></td><td></td><td>See BAR '00B8'.</td><td></td><td>See MICRO 62.</td></tr>
<tr><td>01F8</td><td></td><td></td><td>See BAR '0054'.</td><td></td><td></td></tr>
<tr><td>0248
0348
0458
0518
0778</td><td></td><td></td><td>See BAR '00B8'.</td><td></td><td></td></tr>
<tr><td>08E4</td><td></td><td></td><td>See BAR '0054'.</td><td></td><td></td></tr>
<tr><td>0C24</td><td>B2N2</td><td>KK 201</td><td>Special Op 01 caused clock stop.</td><td></td><td></td></tr>
</table>

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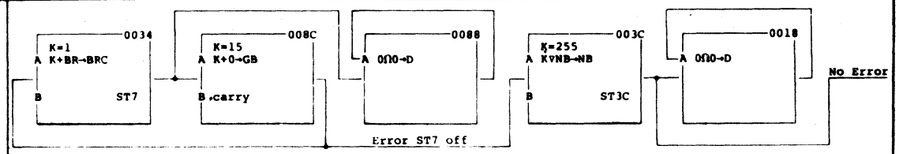
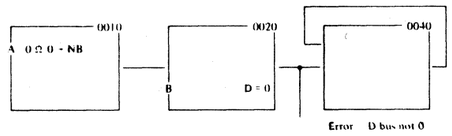
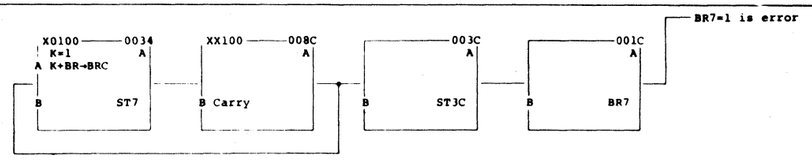
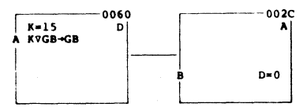
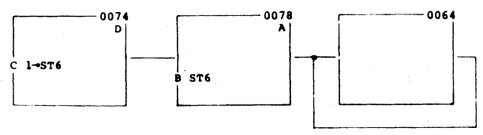
1. Match BAR indication with listing on these pages until a match is found. Take action indicated.
2. Refer to START 900-911 for data flow by card and common card information.
3. Refer to LGND section for logic symbology, voltage levels, etc.

LOOP WORD LIST

BAR (Hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses (Hex)	CAS
0018	B2F2, B1N2, B2L2, B2N2 B2M4		ST3C Branch (CL4) failure at address '003C'. ALU statement K+BR→BRC should have set ST register bit 3 at address '0034'. Carry occurred, but ST3C did not set.	0000–003C	
0028	B1M2, B1P2, B2N2		D=0 Branch failure (CL2) at address '0060'. ALU statement K(FF)⩛NB(FF) →NB at address '0050' should result in D bus=zero. NB register set to 'FF' at address '003C'. Setting of NB register most probable error.	0000–0060	See MICRO 62
0030	B2F2, B2L2, B1P2, B2H2, B2K2, B2T2, B2Q2, B1U4, B2S2		BR6 or 7 Branch (CH or CL10) failure. BR register bit 6 used as branch at address '0080'. BR register bit 7 used as branch at '0038'. ALU statement K(0F)Ω20 →BR at address '0020' should have set BR register to '0F'. Recycle address '0000'–'0080'. Address stop at '0080'. Display BR register, if not '0F', register failed to set. If BR='0F', operate Single Instruction switch. If address goes to '0030', BR6 Branch failed.	BR6 Failure 0000–0080 BR7 Failure 0000–0038	See MICRO 62
0034 0038	B1N2, B1J2, B1H2, B2N2, B2H2		Carry failure.		See MICRO 62
0040 0044	B1N2,B2H2,B2L2,B2P2,B2N2 B1J2, B1H2 B1E2, B1M2, B1L2, B1F2, B2D2, B2E2 B2F2, B1K2		D bus not zero. If NB register contain '00' suspect D = 0 branch logic. If NB not '00', swap B1H2 with B1J2. Re-IMPL. If pattern in NB changes, replace B1H2 or B1J2. If pattern in NB does not change, one of the general purpose registers is placing multiple hot bits on the A or B bus.	0000–0020	
004C	B2F2. B2L2, B2M4		ST7 Branch (CL6) failure. ST register bit 7 was on and caused branch at address '00F0'. Bit 7 should have been off. ALU statement 0Ω20 →ST at address '0078' should have reset the ST register to '00'.	0000–00F0	See MICRO 62
0054	B2L2, B1N2, B2F2		BR7 Branch (CL10) failure. BR7 Branch should not occur at address '001C'. Looping (255 times) from '0034'–'008C' should cause BR register bit 7 to be off at '001C'. BR register should be '00' at entry to '0034'.	0000–001C	
0058	B1M2, B2H2, B1J2, B1P2		D=0 Branch (CL2) failure. D=0 Branch should be on at address '002C'. GC set to '0F' at address'008C'.	0000–002C	
0064	B2M4, B2F2, B2L2		ST6 Branch (CH6) failure. ST register bit 6 should be on at address '0078'. ST register bit 6 set to 1 at '0074'.	0000–0078	

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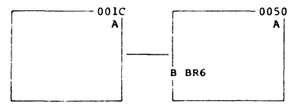
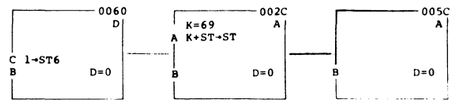
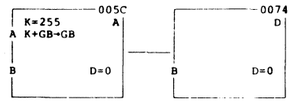
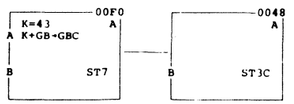
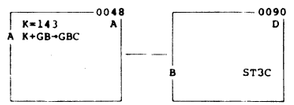
MICRODIAGNOSTIC ERROR CODE DICTIONARY (Hardcore Routine 00)

1. Match BAR indication (hex) with listing on these pages until a match is found. Take action indicated.
2. Refer to START 900-909 for data flow by card and common card information.
3. Refer to LGND section for logic symbology, voltage levels, etc.

LOOP WORD LIST

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses	CAS
0068	B2L2, B1N2, B2F2		BR6 branch (CH10) failure. BR6 branch should not occur at address '0050'. Refer to BAR '0054'.	0000–0050	
0070	B2M4, B2F2, B2N2		D=0 branch (CL2) failure. D=0 branch should be on at address '005C'. ALU statement at address '002C' should cause D-bus to equal '00'. ST register set to 'A9' at address '0080'. ST register bit 3 set to 1 at address '0034'. ST register bit 6 set to 1 at '0060'. ST register should equal 'BB' at entry to '002C'.	0000–005C	
007C	B2L2, B1N2		D=0 branch (CL2) failure. D=0 branch should not occur at address '0074'. GB is '00' at entry to '005C'. ALU statement at address '005C' should cause D-bus to be 'FF'.	0000–0074	
0084	B1N2, B2L2, B2H2, B2P2 B2N2		D=0 branch (CL2) failure. D=0 branch should not occur at address '0044'. ALU statement K(0F)Ω0 →BR at address '0020' should cause D-bus to equal '0F' and prevent D=0 latch from being on at address '0044'.	0000–0044	See MICRO 62
0088	B2F2, B2L2, B2H2, B2P2, B2K2, B2N2		ST7 branch (CL6) failure. ST7 branch should occur at address '0034'. ALU statement K(A9)ΩST →ST at address '0080' should set ST register bit 7 on.	0000–0034	See MICRO 62
008C	B1N2, B2L2, B2H2, B1J2		Carry branch (CH2) failed to occur at '008C'.	Not applicable Run in loop	See MICRO 62
0094	B2F2, B2L2. B2M4		ST3C branch (CL4) failure. ST3C branch should not occur at address '0048'. GB register should be '55' at entry to '00F0'. ST register is reset to '00' at address '0078'.	0000–0048	
0098	B1N2, B2L2, B2F2		ST3C branch (CL4) failure. ST3C branch should occur at address '0090'. GB register equals '80' at entry to '0048'. Carry should occur at address '0048' and set ST register bit 3 on.	0000–0090	
00A4	B2M4, B2F2, B2L2		ST3C branch (CL4) failure. ST3C branch should not occur at address '009C'. ST register bit 3 should be set to '0' by 0 →ST3C statement at address '0090'.	0000–009C	See MICRO 62

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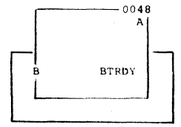
Hardcore Routine 00

1. Match BAR indication (hex) with listing on these pages until a match is found. Take action indicated.
2. Refer to START 900-909 for data flow by card and common card information.
3. Refer to LGND section for logic symbology, voltage levels, etc.

LOOP WORD LIST

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses	CAS
00A8	B1S2, B2S2, B2L2, B2F2, B1N2, B1P2		BTRDY branch (CL8) failure. Failure of IMPL circuitry to properly decode data under micro-program control. SECTR branch recognized OK. Also suspect TG register bits to MPL control circuitry. TG register should equal '90'. May be scoped while looping if TG register OK.		
00C0	B2L2, B1S2, B1T4, A1S2, B2J2, B2F2		SECTR branch (CH) failure. Failure of IMPL circuitry to recognize Sector Pulses under micro-program control.		See MICRO 62
00F8	B2L2, B2F2		ST6 branch (CH6) failure. ST6 branch failure should not occur at address '006C'. ST register should have been reset to '00' at address '0078'.	0000–006C	See MICRO 62

Hardcore Routine 01

LOOP WORD LIST

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses	CAS
0180			Refer to BAR '00C0'.		
0190			Refer to BAR '00A8'.		

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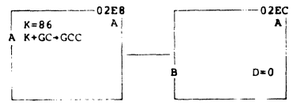
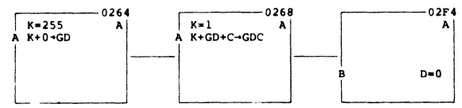
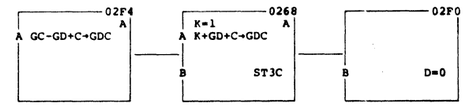
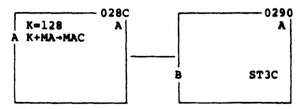
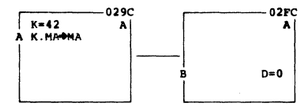
MICRODIAGNOSTIC ERROR CODE DICTIONARY (Hardcore Routine 02)

1. Match BAR indication (Hex) with listing on these pages until a match is found. Take aciton indicated.
2. Refer to START 900-909 for data flow by card and common card information.
3. Refer to LGND section for logic symbology, voltage levels, etc.

LOOP WORD LIST

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses	CAS
0228			Refer to BAR '00A8'.		
0250			Refer to BAR '00C0'.		
0260	GC = '00' B1N2, B2N2, B2L2 GC not '00' B1L2, B1P2		D=0 branch failed to occur at address '02EC'. GC is set to 'AA' at '02E4'. K('56') added to GC at '02E8' should cause D Bus to equal '00' and result in D=0 branch at '02EC'. Stop at address '02EC'.	02E4–02EC	
026C	GD not 'FF' B1F2, B1P2, B2K2, B1N2 GD = 'FF' B1N2, B2N2		D=0 branch erroneously occurred at address '02F4'. Suspect GD not setting to 'FF' at address '0264'. ST3C equals 1 at entry to '0268'. Stop at address '0264'.	02E4–02F4	
0270	GC not '00' B1N2, B1H2, B1J2 GD not '01' B1F2, B1P2, B1N2		D=0 branch failed to occur at address '02F0'. GC='00', GD='01', ST register bit 3 on at entry to '02F4'. Stop at address '02F4'.	02E4–02F0	
0278	ST7 = 1 B2L2 ST7 = 0 B2F2, B2M4, B1P2		ST7 branch failed to occur at address '0280'. ST register is set to '01' at address '02F0'. Stop at address '0280'.	02E4–0280	
0284	ST2= 1 B2L2 ST2 = 0 B2F2, B2M4, B1P2		ST2 branch failed to occur at address '027C'. ST is set to '20' at address '0280'. Stop at address '027C'.	02E4–027C	
0288	B2F2, B2L2, B2M4		ST2 branch erroneously occurred at address '0274'. ST is set to '01' at address '02F0'.	02E4–0274	
0294	B2F2, B2M4, B2L2		ST7 branch erroneously occurred at address '028C'. ST is set to '20' at address '0280'.	02E4–028C	
0298	B1N2, B2F2, B2M4, B2L2, B1E2, B1P2		ST3C branch failure. ST3C branch should occur at address '0290' as a result of carry from ALU OP at address '028C'. MA='FF' at entry to '028C' as result of ALU OP at address '0274'. Set MA register to 'FF' from CE panel. If failure occurs, replace cards B1E2 and B1P2.	02E4–0290	
02A0	B1N2, B1H2, B1J2, B1E2		D=0 branch failure. D=0 branch should occur at address '02FC' as result of ALU OP at '029C'. MA='55' at entry to '029C'.	02E4–02FC	

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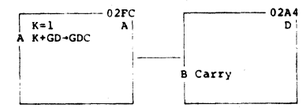
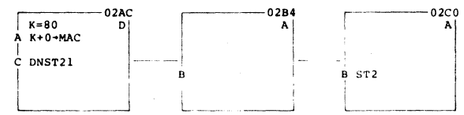
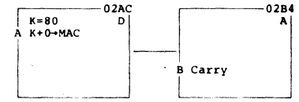
3. Refer to LGND section for logic symbology, voltage levels, etc.

LOOP WORD LIST

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses	CAS
02A8	B2F2, B2M4		ST7 branch failure. ST7 branch should occur at address '02B8' as a result of 1 →ST7 statement at address '02A4'.	02E4–02B8	
02B0	B1N2, B1J2, B2L2		CARRY branch failure. CARRY branch should occur at address '02A4' as result of ALU OP at address '02FC'. GD is set to 'FF' at address '027C'.	02E4–02A4	
02BC	B2F2, B2M4		ST2 branch failure. ST2 branch should not occur at address '02AC' due to 0 →ST2 statement at address '02B8'.	02E4–02AC	
02C4	B2F2, B2M4		ST2 branch failure. ST2 branch should occur at address '02C0' as result of ALU OP and CS statement at address '02AC'. DNST21 sets register bit 2 to a 1 if current ALU OP result is nonzero.	02E4–02C0	
02C8	B1N2, B2L2		CARRY branch failure. CARRY branch should not occur at address '02B4' as result of ALU OP at address '02AC'.		

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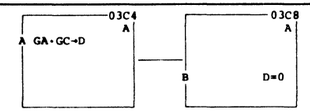
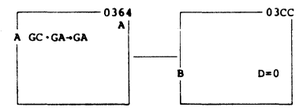
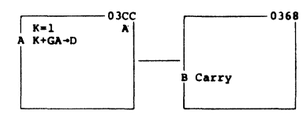
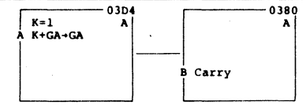
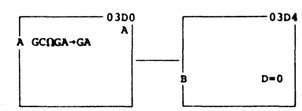
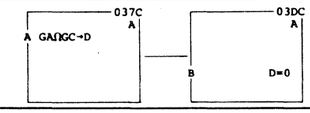
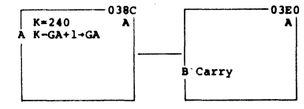
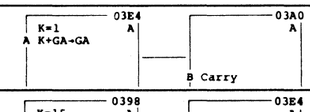
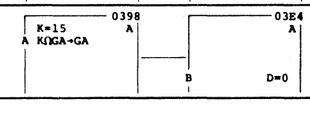
LOOP WORD LIST

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses	CAS
0328			Refer to BAR '00A8'.		
0350			Refer to BAR '00C0'.		
0360	GC not '00' B1L2, B1P2 GC = '00' B1N2, B2L2, B1L2		D=0 branch failure. D=0 branch should occur at address '03C8' as result of ALU OP at '03C4'. GA='FF' and GC='00' at entry to '03C4'. GA is set to 'FF' at '038C' and GC is set to '00' at '03C0'. Address stop at '03C4'.	03BC–03C8	
036C	GC = '00' B1L2, B1P2 GA not 'FF' B1E2, B1P2, B1N2, B1H2, B1J2 GA = 'FF' B1N2, B2L2, B2N2		D=0 branch erroneously occurred at address '03CC'. GC='FF' and GA='FF' at entry to '0364'. GA is set to 'FF' at '03BC'. Register GC is set to 'FF' at '03C8'. Address stop at '0364'.	03BC–03CC	
0370	GA = '00' B1N2, B1J2, B2N2 GA = 'F0' B1H2, B1N2 GC = '00' B1L2, B1P2		CARRY branch failed to occur at address '0368'. GA='FF' at entry to '03CC'. Address stop at '03CC'.	03BC–0368	
0374	B1N2, B1H2, B1J2		CARRY branch failed to occur at address '0380'. GA is set to 'AA' at '0368'. GC is set to '55' at '0378'.	03BC–0380	
0384	GA not '00' B1N2, B2L2, B2N2 GA = '00' B1N2, B1H2, B1J2		D=0 branch erroneously occurred at address '03D4'. GC='55' and GA='AA' at entry to '03D0'. Address stop at '03D4'.	03BC–03D4	
0388	B1N2, B2L2, B2N2		D=0 branch failed to occur at address '03DC'. GC and GA='00' at entry to '037C'.	03BC-03DC	
0390	GA = '00' B1N2, B1J2, B2N2 GA = 'FF' B1N2, B2N2 GA = 'F0' B1N2, B1H2, B2N2		CARRY branch failed to occur at address '03E0'. GA is set to 'F0' at '03DC'. Complement of GA register '0F' is added to constant 'F0' with carry-in at address '038C'. Result should set Carry latch. Address stop at '03E0'.	03BC–03E0	
0394	B1N2, B1H2, B1J2		CARRY branch failed to occur at address '03A0'. GA='FF' at entry to '03E4'.		
03A4	B1N2, B1H2, B1P2		D=0 branch erroneously occurred at address '03E4'. GA='F0' at entry to '0398'.	03BC–03E4	

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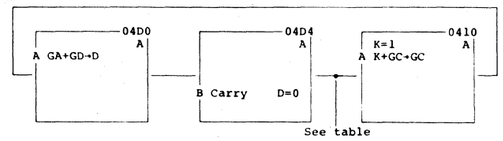
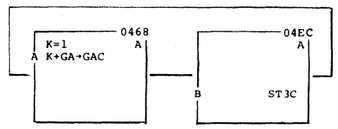
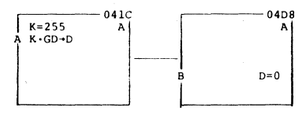
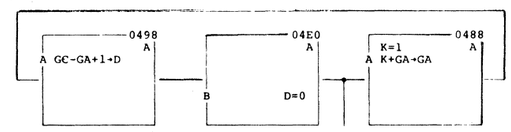
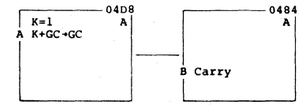
1. Match BAR indication (hex) with listing on these pages until a match is found. Take action indicated.
2. Refer to START 900-909 for data flow by card and common card information.
3. Refer to LGND section for logic symbology voltage levels, etc.

LOOP WORD LIST

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses	CAS
0410	B1N2, B1H2, B1J2, B2L2, B2N2		CARRY and/or D=0 branch failure. D=0 and CARRY branches should occur simultaneously at address '04D4'. GD and GC are initially set to '00'. GA is set to '01'. Loop from '04D0' to '04D4' to '0410' continues until CARRY and/or D=0 occur. Carry / D = 0 / Branch to 0 / 0 / 0410 0 / 1 / 0414 1 / 0 / 0418 1 / 1 / 041C	04D0–0410 04C0–0414 04C0–0418 Normal Branch	
0414			Refer to BAR '0410'.		
0418			Refer to BAR '0410'.		
0438			Refer to BAR '00A8'.		
0468	B1N2, B2F2, B2M4, B2N2		ST3C branch failure. GA is set to '00' at '04A4'. Value of '01' is added to GA until CARRY occurs which should set ST3C.	0468–04EC	
0470			Refer to BAR '00C0'.		
0480	GD not '00' B1F2, B1P2, B1N2 GD = '00' B1N2, B1H2, B1J2		D=0 branch failed to occur at address '04D8'. GD='00' at entry to '041C'. Address stop at '041C'.	04C0–04D8	
0488	B1N2, B2L2 B2N2		D=0 branch failure. Add 2's complement (subtract) did not result in D=0 branch at address '04E0'. GC is set to 'FF' at '0484'. GA is set to '01' at address '04C8'. If branch doesn't occur, loop will be '0498' to '04E0' to '0488' to '0498'. These words will normally loop 257 times and GA will be '01' at exit.	0498–0488	
0490	B1L2, B1P2, B2N2		CARRY branch failed to occur at address '0484'. GC should have been set to 'FF' by loop at address '0410'. Most probable failure is GC register.	04C0–0484	
0498			Refer to BAR '0488'.		

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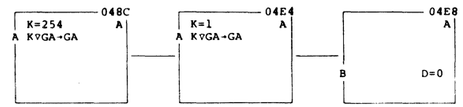
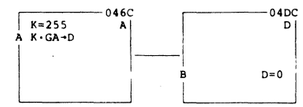
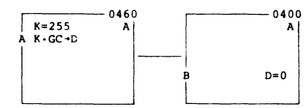
MICRODIAGNOSTIC ERROR CODE DICTIONARY (Hardcore Routine 04)

1. Match BAR indication (hex) with listing on these pages until a match is found. Take action indicated.
2. Refer to START 900-909 for data flow by card and common card information.
3. Refer to LGND section for logic symbology, voltage levels, etc.

LOOP WORD LIST

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses	CAS
04A0	GA = '00' B1N2, B2L2, B2N2 GA not '00' B1E2, B1P2, B1N2, B2H2		D=0 branch failed to occur at address '04E8'. GA='FF' at entry to '048C'. Address stop at '04E8'.		
04A8	B1N2, B1H2, B1J2		D=0 branch failed to occur at address '04DC'. GA is '00' at entry to '046C'.	04C0–04DC	
04B0	B1N2, B1H2, B1J2		D=0 branch failed to occur at address '0400'. GC is '00' at entry to '0460'.	04C0–0400	
04D0			Refer to BAR '0410'.		
04D4			Refer to BAR '0410'.		
04E0			Refer to BAR '0488'.		
04EC			Refer to BAR '0468'.		

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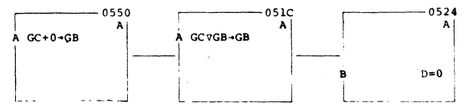
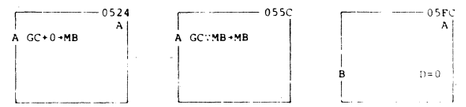
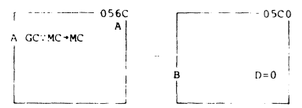
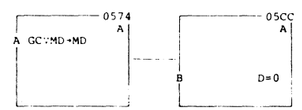
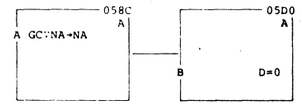
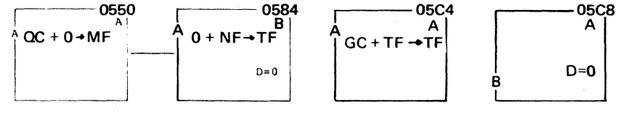
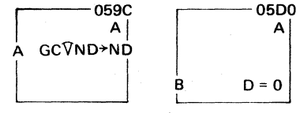
LOOP WORD LIST

1. Match BAR indication (hex) with listing on these pages until a match is found. Take action indicated.
2. Refer to START 900-909 for data flow by card and common card information.
3. Refer to LGND section for logic symbology, voltage levels, etc.

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses	CAS
0528			Refer to BAR '00A8'.		
0558	B1M2, B1P2, B1L2		D=0 branch failed to occur at address '0524'. GC contains a pattern used to test other registers. This pattern will be '00', '55', or 'AA'. GB should be '00'.	0550–0524	
0568	B1M2, B1P2, B1L2		D=0 branch failed to occur at address '05FC'. Refer to BAR '0558' for comment on GC register. MB should='00'.	0550–05FC	
0570	B1L2, B1P2		D=0 branch failed to occur at address '05C0'. Refer to BAR '0558' for comment on GC register. MC should='00'.	0550–05C0	
0588	B1F2, B1P2, B1L2		D=0 branch failed to occur at address '05CC'. Refer to BAR '0558' for comment on GC register. MD should='00'.	0550–05CC	
0590	B1E2, B1P2, B1L2		D=0 branch failed to occur at address '05D0'. Refer to BAR '0558' for comment on GC register. NA should='00'.	0550–05D0	
0598	B1M2, B1P2, B1L2		D=0 branch failed to occur at address '05D4'. Refer to BAR '0558' for comment on GC register. NB should='00'.	0550–05D4	
05A0	B1G2, B1P2, B1L2		D=0 branch failed to occur at address '05C8'. GC contains pattern used to test the NF and TF register. The NP should contain the pattern, and the TF should be '00'.	0550-05C8	
05A8	B1F2, B1P2, B1L2		D = 0 branch failed to occur at address '05D4'. Refer to BAR '0558' for comments on GC register. NB should = '00'.	0550-05DC	
05B0			Refer to BAR '00C0'.		

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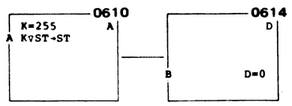
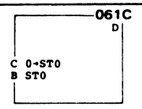
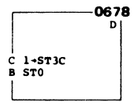
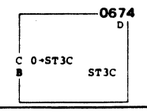
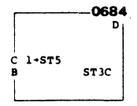
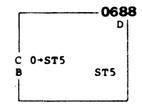
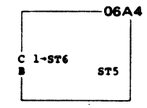
MICRODIAGNOSTIC ERROR CODE DICTIONARY (Hardcore Routine 06)

1. Match BAR indication with listing on these pages until a match is found. Take action indicated.
2. Refer to START 900-911 for data flow by card and common card information.
3. Refer to LGND section for logic symbology, voltage levels, etc.

LOOP WORD LIST

BAR (Hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses (Hex)	CAS
0618	B2F2, B1P2		ST register failure. D=0 branch should occur at address '0774'. ST register is set to 'FF' at address '0610'. The ST register is then exclusive or'ed with a K value of 'FF' which should result in D bus=0.	0610–0614	
0624	B2F2, B2L2		BR Register failure. Bit 5 should be off.	0690–0624	
0628	B2F2, B2L2, B2T2, B1U4		BR Register failure. Bit 4 should be off.	0690–0628	
0640	B2L2		SP OP 7 Active	063C–0640	
0670	B2M4, B2N2, B2F2		ST0 branch failure. ST0 should be on at entry to address '061C'. ST0 is set to '1' at address '0614'.	0610–061C	
067C	B2M4, B2N2, B2F2		ST0 branch failure. ST0 should be off at address '0678'. ST0 is reset to '0' at address '061C'.	0610–0678	
0680	B2M4, B2N2, B2F2		ST3C branch failure. ST3 should be on at address '0674'. ST3 is set to '1' at address '0678'.	0678–0674	
068C	B2M4, B2N2, B2F2		ST3C branch failure. ST3 should be off at address '0684'. ST3 is reset at address '0674'.	0674–0684	
0694	B2F2, B2L2		BR Register failure. Bit 1 should be off.	0600–0694	
0698	B2F2, B2L2		BR Register failure. Bit 0 should be off.	0600–0698	
06A0	B2M4, B2N2, B2F2		ST5 branch failure. ST5 should be on at entry to address '0728'. ST5 is set to '1' at address '0684'.	0684–0688	
06AC	B2M4, B2N2, B2F2		ST5 branch failure. ST5 should be off at address '06A4'. ST5 is reset to '0' at address '0688'.	0688–06A4	

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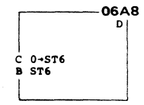
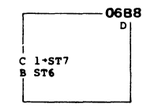
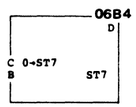
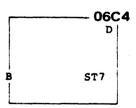
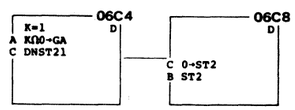
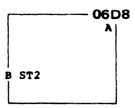
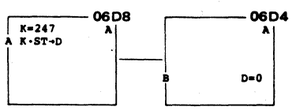
1. Match BAR indication with listing on these pages until a match is found. Take action indicated.
2. Refer to START 900-911 for data flow by card and common card information.
3. Refer to LGND section for logic symbology, voltage levels, etc.

LOOP WORD LIST

BAR (Hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses (Hex)	CAS
06B0	B2M4, B2N2, B2F2		ST6 branch failure. ST6 should be on at entry to address '06A8'. ST6 is set to '1' at address '06A4'.	06A4–06A8	
06BC	B2M4, B2N2, B2F2		ST6 branch failure. ST6 should be off at address '06B8'. ST6 is reset to '0' at address '06A8'.	06A8–06B8	
06C0	B2M4, B2N2, B2F2		ST7 branch failure. ST7 should be on at entry to address '06B4'. ST7 is set to '1' at address '06B8'.	06B8–06B4	
06CC	B2M4, B2N2, B2F2		ST7 branch failure. ST7 should be off at address '06C4'. ST7 is reset to '0' at address '06B4'.	06B8–06C4	
06D0	B2M4, B2N2, B2F2, B1N2		ST2 branch failure. ST2 should be on at entry to address '06C8'. ST2 is set to '1' at address '0604' by DNST21.	0604–06C8	
06DC	B2M4, B2N2, B2F2		ST2 branch failure. ST2 should be off at address '06D8'. ST2 is reset to '0' at address '06C8'.	06C4–06D8	
06E0	B2M4, B2N2, B2F2		ST register failure. D=0 branch should be off at address '06D4'. All ST register bits are set and then reset. No bits should be on in the ST register at this time. If ST4 is on, suspect the external set to ST4.	0600–06D4	

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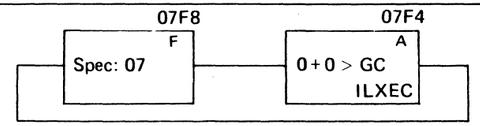
MICRODIAGNOSTIC ERROR CODE DICTIONARY (Hardcore Routine 07 and 08)

1. Match BAR indication with listing on these pages until a match is found. Take action indicated.
2. Refer to START 900-911 data flow by card and common card information.
3. Refer to LGND section for logic symbology, voltage levels, etc.

Hardcore Routine 07

LOOP WORD LIST

BAR (Hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses(Hex)	CAS
0738			Refer to BAR '00C0'		
07A0			Refer to BAR '00C0'		
07C8			Refer to BAR '00C0'		
07F4 07F8 07FC	B2L2, B2T2		1. The pgm. is attempting to display 0800 and is waiting entry of control store size. Place enter/display sw to pgm data entry/display. Refer to START 25. 2. ILXEQ branch failed. Refer to PANEL 30.		

Hardcore Routine 08

LOOP WORD LIST

BAR (Hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses (Hex)	CAS
0800	B1G2, B1U4, B2N2	INST 20 Step 6.	Hard core routine "08" (Control Storage scan) reads configuration card (B1G2) to determine storage size. If B1G2 is defective or plugged wrong, or Spec:0C fails, storage scan will overlay the program and cause this 0800 loop.		
0830			Refer to BAR '0890'		
0884		FSI 32	If BAR='0884', then MC and MD registers contain a pattern which can be compared against storage read bus to determine incorrect bit(s). Set Mode switch to Storage Display. Operate low order Address Data Entry switch to 0, 1, 2, and 3. As the switch is rotated, storage read bus bytes 0 through 3 will be displayed in the Register/Storage Display lamps. Compare as follows: Byte 0 / MC Reg | Byte 1 / MC Reg | Byte 2 / MD Reg | Byte 3 / MD Reg Go to FSI 32 and determine defective array card.	0884-08C4	
0888	B3C2, B2G2, B2H2, B2N2, B2M4, B2P2	FSI 32	Storage read error. MC register contains the pattern for bytes 0 and 1. MD register contains the pattern for bytes 2 and 3. Contents of NA and NC contain the address in control storage where the read error occurred. Example: NA='09', NC='10', address in error - '0910'. Check actual control store against expected bytes. Go to FSI 32 and determine failing array card(s).		
0890	B1E2, B1P2, B2N2, B2L2		D=0 branch failure. A value of '05' is placed in the GA register. A value of 'FF' is then added to GA, effectively subtracting 1 from GA on each loop. After five such adds, the GA register and the D-bus='00'.		
0894		FSI 32	If BAR='0894', then MA and MB registers contain a pattern which can be compared against the SA, SB, SC, and SD registers. Look for bad parity and correct patterns in the S registers. This is a write error. Compare as follows: MA Reg / SA Reg | MA Reg / SB Reg | MB Reg / SC Reg | MB Reg / SD Reg Go to FSI 32 and determine defective array card.	0880-0894	

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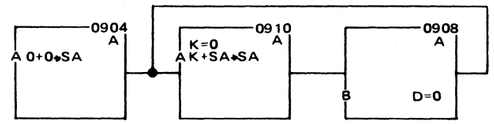
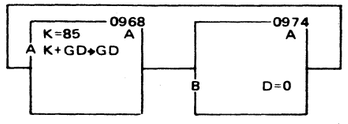
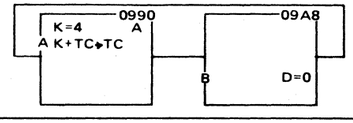
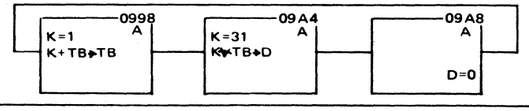
1. *Match BAR indication with listing on these pages. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*
3. *Refer to LGND section for logic symbology, voltage levels, etc.*

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses	CAS
0908	GD Values Hex Reg Card — Card B1P2 60 SA B2D2 B2G2 B2H2 61 SB B2E2 62 SC B2D2 63 SD B2E2 64 GB B1M2 65 GA B1E2 67 NA B1E2 68 MB B1M2 69 TA B1E2 6A TD B1F2 6B MA B1E2 6C MD B1F2 6D GC B1L2 6E BR B2F2 6F MC B1L2 74 ND B1F2 75 NC B1L2 76 NB B1M2 B1P2	CTRL 118	Register test failure. Suspect a register not setting. K (constant) is changed at address '0910' by the program. First time through for each register, value is '00'. Each time thereafter, '55' is added to the register until D=0 branch occurs. If D=0 branch does not occur, GD register contains a value which represents the register being tested. Refer to table at left. Hex Reg Card Card 78 GF B1G2 B1P2 79 GE B1K2 B1P2 7A NF B1G2 B1P2 7B NE B1K2 B1P2 7C TF B1G2 B1P2 7D TE B1K2 B1P2 7E MF B1G2 P1P2 7F ME B1K2 B1P2	0900-09AC	
0910			Refer to BAR '0908'.		
0920			Too many errors (16 Read Data checks or 3 consecutive seek errors) while overlaying address '00XX' and '01XX'. Refer to '00F4' (MICRO 65).		
0940	B2F2, B2M4, B1P2		ST6 branch failure. ST register bit 6 should be set by the 1→ST6 statement at address '0940'. This results in an ST6 (CA branch) at address '0964'.		
0960			Refer to BAR '0940'.		
0964			Refer to BAR '0940'.		
0968	B1F2, B1P2, B2N2		Test of GD register failed. A constant of '55' is added to GD in a loop until D=0 branch occurs.		
0970			Refer to BAR '0940'.		
0974			Refer to BAR '0968'.		
0990	B1L2, B1P2, B2N2	CTRL 118	TC register failed. A constant of '04' is added to TC register until D=0 branch occurs.		
0998 09A4 09A8	B1M2, B1P2, B1N2	CTRL 118	Test of TB register failed. A constant of '01' is added to TB. TB is exclusive ORed with '1F' until D=0 branch.		
09A0			Refer to BAR '0990'.		
09C0	B2N2				

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1. *Match BAR indication with listing on these pages. Take action indicated.*
2. *Refer to START 900-909 for data flow by card and common card information.*
3. *Refer to LGND section for logic symbology, voltage levels, etc.*

BAR (hex)	Possible Failing Replaceable Units			Reference	Error Description and Comments	Recycle Addresses	CAS
0A28	*B1F2	B1R2	B1D2		Hot Check 2 Condition. Special Operation 13 was performed, which gates Control Interface checks into the ND register. No checks should be present at this time. Replace the cards as required. **Scope Procedure:** When loop word is reached, stop the clock, then recycle the words shown (see PANEL 16 for recycle procedure). Next, scope the appropriate hot line (see table below) at the input of the ND register (RG403).		0A08 0 → TD 0A0C 0A10 SPEC: 0D
0A30	*B1F2	B1R2	B1D2				
0A38	*B1F2	B1R2	B1M2				
0A40	*B1F2	B1Q2					
0A48	*B1F2	B1D2	B1R2				
0A50	*B1F2	B1R2	B1M2				
0A58	*B1F2	B1R2					

Loop word	ND Bit	Name
0A28	6	Transfer Check
0A30	5	Bus Out Parity Check
0A38	4	Tag Bus Parity Error
0A40	3	Unexpected End
0A48	2	Buffer (Bus In) Parity Error
0A50	1	Select Active Check
0A58	0	Controller Check

BAR (hex)	Possible Failing Replaceable Units			Reference	Error Description and Comments	Recycle Addresses	CAS
0A60	B1R2	*B1B2	B1Q2, B1F2		Hot Control Interface Inbound Line. Special Op 13 was performed with TD register bit 1=1. This gates certain control interface inbound lines into the ND register. All inbound lines should be inactive at this time (all control modules must be powered off to run hardcore tests). For loop words '0A60' through '0A88', replace the cards shown for the loop word. **Scope Procedure** When loop word is reached, stop the clock, then recycle the words shown (see PANEL 16 for recycle procedure). Next, scope the appropriate hot line at the input to the ND register (RG403). See table below. *This is a multiple usage card. Refer to START 900-909 for common part numbers.		0A00 K=64 K → TD 0A04 SPEC: 0D
0A68	B1R2	*B1C4	B1F2				
0A70	B1R2	*B1C4	B1F2				
0A78	B1R2	B1D2	*B1B2 B1F2				
0A80	B1R2	*B1B2	B1F2				
0A88	B1R2	*B1C4					

Loop word	ND Bit	Name
0A60	6	Tag Valid
0A68	5	Check End
0A70	4	Normal End
0A78	2	Sync In
0A80	1	Select Active
0A88	0	Select Alert 1

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (Hardcore 0A Loop Word List)

1. *Match BAR indication with listing on these pages. Take action indicated.*
2. *Refer to START 900-909 for data flow by card and common card information.*
3. *Refer to LGND section for logic symbology, voltage levels, etc.*

BAR (hex)	Possible Failing Replaceable Units			Reference	Error Description and Comments		Recycle Addresses	CAS
0A90	B1Q2	B1D2	*B2L2		Both MC-6 and MC-7 Branches failed	Scope procedure: Recycle from microword '0A00' to '0AC0' (See PANEL 16 for recycle procedure), then scope the failing branch condition per DE306.	0A00 – 0AC0	0A00 — // — 0A14 K=3 K→MC — // — 0AC0 0→MC MC6 MC7 Turn on MC register bits 6 and 7 — Both branches should be active
0A94	B2L2	B1Q2	*B1L2		MC-6 Branch failed			
0A98	B2L2	B1Q2	*B1L2		MC-7 Branch failed			
0AA4	B2L2	B1Q2	*B1L2		Hot MC-7 Branch Condition	Scope Procedure: Recycle from microword '0A84' to '0AC0' (See PANEL 16 for recycle procedure), then scope the hot branch condition per DE306. *Note: To recycle the words shown, set ACR to '0AC0' and set IAR to '0A8C'. Set switches to '0A84' and operate Start switch.*	0A84 – 0AC0	0A84 K=3 K→ TC — // — 0A8C — // — 0AC0 0→MC MC6 MC7 Set Data Response state — Both branches should be off
0AA8	B2L2	B1Q2	*B1L2		Hot MC-6 Branch Condition			
0AAC	B2L2	B1Q2	*B1L2		Both MC-6 and MC-7 Branches hot			
0AB4	B2L2	B1R2	B1D2		Hot CL-15 Branch Condition	Scope Procedure: Loop on microword '0AA0' (See PANEL 16 for recycle procedure), then scope CL-15 per DE306.		
0ACC	A1S2	B2L2	B1U4		Hot ILACT Branch Condition - Scope procedure: Recycle the microwords shown (PANEL 16), then scope ILACT per GK702.		0A00 – 0AB0	0A00 — 0AB0 SPEC: 14 Special Op 20 (should reset Inline Active).
0AD0	A1S2 A1R2	B2L2	B1U4		ILACT Branch Failed - Scope procedure: Recycle the following microwords (PANEL 16), then scope ILACT per GK702.		0A00 – 0AB8	0A00 — 0AB8 SPEC: 13 Spec Op 19 should set Inline Active
0ADC	A1S2	B1U4			ILACT Branch did not reset – Scope procedure – same as loop word '0ACC'.			
0AEC	B2L2 B1M2	B2T2	*B1B4		Hot ILXEQ Branch - Scope procedure: Recycle the microwords shown (PANEL 16), then scope BR5 branch condition per DE301. *Note: This loop will also occur if a device on the control interface is powered on and the Execute switch has been operated. The device must be powered off to reset. If this loop word occurs only when the wraparound cable is installed, suspect B1C4, B1M2.*		0A00 – 0AC8	0A00 — 0AD8 SPEC: 07 — 0AC8 ILXEQ Branch should be off
					*This is a multiple usage card. Refer to START 900-909 for common part numbers.			

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1. *Match BAR indication with listing on these pages. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*
3. *Refer to LGND section for logic symbology, voltage levels, etc.*

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments		CAS
0B0C	A1S2, B2L2	**CHL-I 30**	BOPAR branch active - The BOPAR (Bus Out Parity Check) branch should be off at initial check time. When sampled, it was found active.		
0B14	A1M2, B1Q2, B2L2		SELTD branch active - The SELTD (Selected) branch should be off at initial check time. When sampled, it was found active.		
0B1C	A1U2, A1M2, A1Q2, B2L2	**CHL-I 145**	CUEND branch for channel A is on - The CUEND (Control Unit End) branch for channel A should be off at initial check time. When sampled it was found active.		
0B28	A1M2, A1U2, B1Q2		ADDRO branch is on - The ADDRO (Address Out) branch should be off at initial check time. When sampled, it was found active.		
0B2C	A1M2, A1R2, B2L2, A1U2		COMMO branch is on - The COMMO (Command Out) branch should be off during the initial check. When sampled, it was found active.		
0B34	A1P2, A1M2, A1U2	**CHL-I 145**	CUEND branch for channel B is on. The CUEND (Control Unit End) branch for channel B should be off at initial check time. When sampled, it was found active. **A1T2 plugged wrong.**		
0B3C	A1R2, B1R2, B2L2, A1D2, A1T2	**CHL-I 180**	CHAN B branch is on. No attempts have been made to select either channel. The machine should be in neutral status and the channel B branch should be off. Note: Check plugging on A1T2.		
0B48	A1R2, A1M2	**CHL-I 150**	SUPPO branch is on - The SUPPO (Suppress Out) branch should be off during the initial check. when sampled. it was found active.		
0B4C	A1T2, A1N2, B2L2, A1M2, A1L2, A1S2, B2Q2, B1Q2	**PANEL 50**	Check 2 branch is on - The Check 2 branch should be off during the initial check. When sampled, it was found active.		
0B54	A1S2, B2L2	**CHL-I 180**	SERVO branch is on - The SERVO (Service Out) branch should be off at initial check time. When sampled, it was found active.		
0B5C	A1U2, A1M2, B2L2	**CHL-I 140**	HLTIO branch is on - The HLTIO (Halt I/O) branch should be off during the initial check. When sampled, it was found active.		
0B64	A1U2, A1M2. A1K2	**CHL-I 145**	CUEND branch for channel C is on - The CUEND (Control Unit End) branch for channel C should be off at initial check time. When sampled, it was found active.		
0B78	A1R2, B2L2	**CS104**	X CHAN (Channel C) is on - The X channel branch should be off at initial check time. When sampled, it was found active.		
0B7C	A1R2, B2L2	**CS104**	X CHAN (Channel D) is on - The X channel branch should be off at initial check time. When sampled, it was found active.		
0B84	A1U2, A1M2, A1J2	**CHL-I 145**	CUEND branch for channel D is on - The CUEND (Control Unit End) branch for channel D should be off at initial check time. When sampled, it was found active.		
0B90	A1T2, B1E2	**CHL-I 155**	Buffer Parity check - A buffer parity error was detected during the initial check.		
0B98	A1T2, A1N2, B1E2	**CHL-I 185**	IFCCHK channel A is on - The IFCCHK (Interface Control Check) for channel A should be off during initial check. When sampled, it was found active.		

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (Hardcore Routine 0B)

1. *Match BAR indication with listing on these pages. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*
3. *Refer to LGND section for logic symbology, voltage levels, etc.*

BAR (hex)	Possible Failing Replaceable Units	Reference	Error Description and Comments	Recycle Addresses	CAS
0BA0	A1T2, A1N2, B1E2	CHL-I 185	IFCCHK channel B is on - The IFCCHK (Interface Control Check) for channel B should be off during initial check. When sampled, it was found active.		
0BA8	A1T2, A1S2		Channel Transfer Check - The Channel Transfer Check should be off at initial check time. When sampled, it was found active.		
0BB0	B1E2, B1R2, A1T2	PANEL 50	Control Interface Check 2, Controller Check. NA register bit 4 should be off at this time.		
0BB8	B1E2, B1Q2, A1T2	CTL-I 120	Control Interface Load S Registers Check-S Register Check should be off at this time.		
0BC0	B1E2, B1Q2, A1T2	CTL-I 120	Control Interface Compare Assist Check - Compare Assist Check should be off at this time.		
0BD4	A1U2	CHL-I 140	XFER branch is on - The Channel Write Control was set, then the XFER branch was sampled. It was found to be on when it should have been off.		
0BDC	A1U2, B1L2	CHL-I 145	BFRDY branch is on. The Channel Write Control was set, then the BFRDY (Buffer Ready) branch was sampled. It was found to be on when it should have been off.		
0BE0	A1U2, B1L2, B2L2, B2Q2	CHL-I 140	XFER branch is off - The Channel Read Control was set, then the XFER branch was sampled. It was found to be off when it should have been on.		
0BE8	A1U2, B1L2, B2L2, A1S2, A1M2, B2P2, B1P2	CHL-I 145	BFRDY branch is off - The Channel Read Control was set, then the BFRDY (Buffer Ready) branch was sampled. It was found to be off when it should have been on.		
0C10 0C14 0C18	B2B2, B2T2, B2C2, B2N2 B1U4		Hardcore tests have been successfully completed. The program is attempting to display '0F0F'. Place Enter/Display switch in Program Data Entry/Display position; then return to START 25.		

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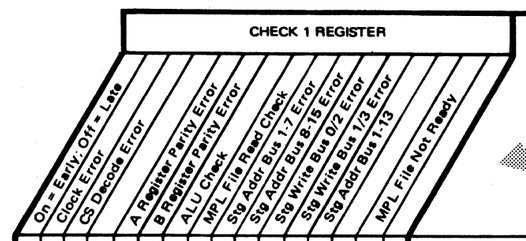
HARDCORE CHECK 1 ANALYSIS

Hardcore routines indicate that an error has been detected in one of three ways:

1. Clock stopped and check-1 error.
2. A single word loop.
3. Program stop.

The following pages (MICRO 150 through MICRO 174) are used to locate the failing unit when the failure is indicated by clock stopped and check-1 error.

Compare the check-1 register contents with the bit pattern shown on the left side of these pages. When a match is found, follow the instructions given in the Action Required column. BAR at the time of error detection is used to isolate the failing unit.



1. *Match check 1 register indication with pattern at left. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*

ERROR DESCRIPTION	ACTION REQUIRED	FIELD REPLACEABLE UNITS in order of probability of failure			REFERENCE
Any Bit Pattern					
	A Check 1 register failure can be associated with any of its bits (0-14). Proceed to matching Check 1 register pattern and take corrective action. If problem is not resolved by that action, replace Check 1 register (B2Q2).	B2Q2			PANEL 40
	Check 1 latch turned on but no bit set in Check 1 register. If Check 1 register parity is okay, suspect Check 1 register card (B2Q2).	B2Q2	B2N2	B2M2	PANEL 40
	If Check 1 register parity is not okay, suspect following: a. Check 1 register parity 0-7 bad b. Check 1 register parity 8-15 bad	B2B2	B2T2		PANEL 40
		B2C2	B2T2		PANEL 40
Clock error	Control unit clock error. Refer to FSI section, Fault Symptom Code '31XX'.	B2N2	B2M2		KK201
CS Decode error	CS field or Status register set error. Also suspect trilead (+ Set Storage Read Latches — KK205)	B2M4	B2K2	B2N2	DE201
		B1P2	B1N2		
CS Decode error and A Register Parity error	Error detected while gating CK field to the A register. If card replacement does not correct problem, suspect trileads for byte 0 from storage board to B2 board (trileads shown on FSI 33).	B2K2			DE201
		*Multiple usage card			

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HARDCORE CHECK 1 ANALYSIS

CHECK 1 REGISTER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
On = Early, Off = Late	Clock Error	CS Decode Error	A Register Parity Error	B Register Parity Error	ALU Check	MPL File Read Check	Stg Addr Bus 1-7 Error	Stg Addr Bus 8-15 Error	Stg Write Bus 0/2 Error	Stg Write Bus 1/3 Error	Stg Addr Bus 1-13	MPL File Not Ready			

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

1. *Match Check 1 register indication with pattern at left. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	ERROR DESCRIPTION	ACTION REQUIRED	FIELD REPLACEABLE UNITS in order of probability of failure			REFERENCE
0	0	0	0	1												A-register parity error.	A. If BAR = '0000' — This indicates an A-bus failure (hot bus bit) or A-register gating failure as no register is gated to the A-bus at address '0000'. Go to Manual Registers test on START 80.	B2H2	B1J2		RA201
																	B. If BAR = '0004' — TB register is gated to the A-bus. TB register should be '00' with good parity. Replace cards. If it still fails, go to START 80.	B1M2*	B1P2	B2S2	
																	C. If BAR = '0020' — A constant of '0F' is gated to BR register. Replace cards. If it still fails, display BR to determine failing bit. Go to ALD and scope while recycling address '0020'.	B2K2 B2H2	B1H2*	B1N2	
																	D. If BAR = '00B0' — A constant of '80' is gated to TG register. Replace cards. If it still fails, display TG to determine failing bit. Go to ALD and scope while recycling address '00B0'.	B2K2	B1J2*	B1N2 B1H2*	
																	E. If BAR = '0118' thru '0178' — Match BAR with table at right. If match is found, the register listed was the register gated onto the A bus when failure was detected. Replace listed cards. If replacement does not fix, go to START 80.				
																	F. If BAR = None of the above — Go to START 80 and perform Manual Register test. If no failure go to FSI section, Fault Symptom Code '3508'.				

BAR	Register	Card Replacement Order			
0118	TD	B1F2*	B1P2	B1H2	B1J2
0120	MD	B1F2*	B1P2		
0128	ND	B1F2*	B1P2		
0130	GC	B1L2*	B1P2		
0138	TC	B1L2*	B1P2		
0140	MC	B1L2*	B1P2		
0148	NC	B1L2*	B1P2		
0150	GA	B1E2*	B1P2		
0158	TA	B1E2*	B1P2		
0160	MA	B1E2*	B1P2		
0168	NA	B1E2*	B1P2		
0170	MB	B1M2*	B1P2		
0174	GB	B1M2*	B1P2		
0178	NB	B1M2*	B1P2		

*Multiple usage card

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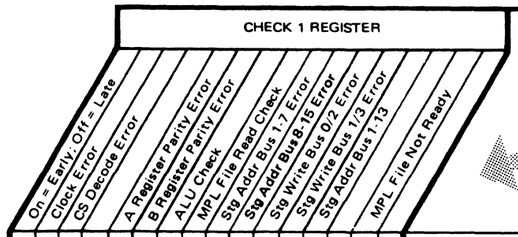
HARDCORE CHECK 1 ANALYSIS



BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

1. *Match Check 1 register indication with pattern at left. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*

ERROR DESCRIPTION

B-register parity error

ACTION REQUIRED

A. If BAR = '0000' or '0004' — This indicates a B-bus failure (hot bus bit) as no register is gated to B-bus at address '0000' or '0004', Go to Manual Registers Test on START 80. If SA, SB, SC, or SD is out of parity when recorded on START 50, suspect external input gate to that register.

B. If BAR is listed in table at right, swap suspect card from table with a common type card, if possible, and rerun tests. If cards do not correct problem, suspect trilead. See ALD RA202 for logic.

C. If BAR = '07F0' — This indicates bad parity from the configuration card, B1G2. See INST 20, step 6, to check jumpers. If jumpers are correct, replace B1G2.

FIELD REPLACEABLE UNITS in order of probability of failure

REFERENCE

RA202

BAR	Register	Card Replacement Order			
0008	SA	B2D2*	B1H2 B1L2 B1F2	B1J2 B2J2 B1M2	B1N2, B1G2, B1K2 B2E2, B2F2,B1E2
0010	NB	B2H2			
002C	ST	B2F2	B1N2		
0034	BR	B2F2	B1H2*	B1N2	B2J2, B1G2, B1J2
0038	ND	B2F2	B1H2*	B1N2	B2J2, B2N2
003C	NB	B1M2*	B1J2*	B1N2	B1P2
0060	GB	B1M2*			
0090	SC	B2D2			
009C	SD	B2E2*			
00A0	SB	B2E2			
011C	MD	B1F2*			
0124	ND	B1F2*	B1P2		
012C	GC	B1L2*	B1H2*	B1N2	B1P2
0134	TC	B1L2*	B1J2*	B2J2	B1P2
013C	MC	B1L2*	B2N2	B1P2	
0144	NC	B1L2*	B1P2		
014C	GA	B1E2*	B1N2		
0154	TA	B1E2*			
015C	MA	B1E2*			
0164	NA	B1E2*	B1P2		
016C	MB	B1M2			
017C	TB	B1M2*			
0184	GD	B1F2*	B1N2		
01E0	SD	B2E2*			
01E4					
01E8					
01EC	BR	B2F2			
01F8	TD	B1F2*			
0268	GD	B1F2*			
028C	MA	B1E2			
0584	NF	B1G2	B1N2		
058C	TF	B1G2	B1U4		
0610	ST	B2F2			
08B4	SA	B2G2	B2D2		
08B8	SB	B2J2			
08BC	SC	B2H2			
08C0	SD	B2L2			
08F8	NF	B1G2			
0910	SA	B1K2	B1P2		
08F8	NA	B1E2	A1T2	B1Q2	

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HARDCORE CHECK 1 ANALYSIS

CHECK 1 REGISTER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
On = Early, Off = Late	Clock Error	CS Decode Error	A Register Parity Error	B Register Parity Error	ALU Check	MPL File Read Check	Stg Addr Bus 1-7 Error	Stg Addr Bus 8-15 Error	Stg Write Bus 0/2 Error	Stg Write Bus 1/3 Error	Stg Addr Bus 1-13	MPL File Not Ready			

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

1. *Match Check 1 register indication with pattern at left. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	ERROR DESCRIPTION	ACTION REQUIRED	FIELD REPLACEABLE UNITS in order of probability of failure			REFERENCE
0	0	0	0	0	1											B-register parity error (Continued)	D. If BAR = '0A0C' (1) Suspect external ND register input. (2) Scope while recycling address '0A0C'.	B1R2	B1Q2	B1F2	RA202
																	E. If BAR=none of the above Go to START 80 and perform Manual Registers test. If no failure, go to FSI section, Fault Symptom Code '3504'.				
0	0	0	0	0	0	1										ALU Check	A. Enter 'FF', '00', and '01' into a register using CE Panel. If incorrect parity, picked or dropped bit(s) resulted, also suspect Data Entry switches, SM955.	B1N2	B2T2	B2S2	RA303
																					RA304
																	B. If BAR = '0000'; (1) Suspect hot checking circuit or hot bit from ALU cards. D bus should be '00' at this time.				RA303
																	(2) Refer to ALD, recycle address '0000' in Check Bypass mode and scope ALU sum bit inputs to D bus card.				
																	(3) If hot bit found in bits 0-3. →	B1J2	B1N2		
																	(4) If hot bit found in bits 4-7. →	B1H2	B1N2		
																	(5) Either hot checking circuit or P bit failure. →	B1N2			
																	C. If none of the above correct problem, go to FSI section, Fault Symptom Code '3502'.				
0	0	0	0	0	0	0	1	0	0	0	0	0	0			MPL File Read Check	MPL Read Parity Error. Go to START 65, entry B.				

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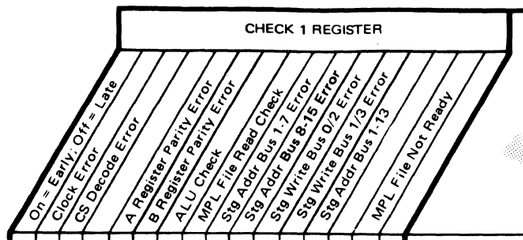
HARDCORE CHECK 1 ANALYSIS



BIT
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

1. *Match Check 1 register indication with pattern at left. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0		1							

ERROR DESCRIPTION: Stg Addr Bus 1-7 error

BAR (Hex)	DAR (Hex)	Register Value (Hex)
0014	01(NB)	NB contains DAR low byte
0114	02(NB)	
0220	03(GD)	
0320	04(GD)	
0430	05(GD)	
0578	06(GD)	
057C	07(GD)	
0718	07(NB)	NB=4C
0730	xx(GD)	xx-decode word; GD=00-FC
0734	07(NB)	NB=30
0764	07(NB)	NB=30
07E4	07(NB)	NB=4C
0884	(NA)(NC)	NA=02-3F; NC=00-FC
0894	(NA)(NC)	NA=02-3F; NC=00-FC
08A8	08(NB)	NB=84/94

ACTION REQUIRED	FIELD REPLACEABLE UNITS in order of probability of failure			REFERENCE
A. If DAR parity incorrect, go to card replacement. Otherwise, go to B.	B2K2	B2J2		RL205
B. Compare recorded BAR value to table, if a comparison is found go to card replacement. Otherwise, go to C.	B2K2	B2J2	B2N2	RL205
C. Set IAR to '7FFC', '0000', and '0404'. If incorrect parity, picked bits, or dropped bits result, go to D. If correct operation go to card replacement. If card replacement does not fix problem go to D.	B2K2 B2H2	B2N2 B2L2	B2T2	RL205
D. Set ACR to '7FFC', '0000', and '0404'. If incorrect parity, picked bits or dropped bits result, suspect one of the two high order rotary switches or display card B2B2. Otherwise, go to card replacement.	B2K2	B2T2		RL205
E. If none of above correct problem, recycle using address from BAR. Refer to ALD for logic and theory, and scope. Cards that can cause problem are listed.	B2K2 B2J2	B2N2 B2T2	B2S2 B2H2	RL205

0	0	0	0	0	0	0		0	1						

ERROR DESCRIPTION: Stg Addr Bus 8-15 error

ACTION REQUIRED	FIELD REPLACEABLE UNITS in order of probability of failure			REFERENCE
A. If DAR parity incorrect, go to card replacement. Otherwise, go to B. If necessary to scope, refer to table under B above, under BAR heading; if failing BAR address is found then the register being gated to DAR low is shown. The value in the register should have been in DAR low at time of failure. Suspect trileads from B1H2, J2, and N2 to DAR Low (B2H2).	B2H2	B2S2	B2L2	RL104
B. Compare recorded BAR to table under B above; if acomparison is found, register listed in parentheses under DAR contains value which should have been in DAR low at time of failure. Suspect trileads from B1H2, J2 and N2 to DAR low (B2H2). Otherwise, go to C.	B2H2			RL104
C. Set IAR to '7FFC', '0000', and '0404', If incorrect parity, picked bits or dropped bits result, go to D. If correct operation go to card replacement.	B2H2	B2N2	B2T2 B2L2	RL104
D. Set ACR to '7FFC', '0000', '0404'. If incorrect parity, picked bits or dropped bits result, suspect one of the two low order rotary switches or display card B2C2. Otherwise, go to card replacement.	B2H2	B2T2		RL104
E. If none of above correct problem, go to FSI section, Fault Symptom codes '3440', and '3448'.				

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HARDCORE CHECK 1 ANALYSIS

CHECK 1 REGISTER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
On = Egriv_Off = Late	Clock Error	CS Decode Error	A Register Parity Error	B Register Parity Error	ALU Check	MPL File Read Check	Stg Addr Bus 1-7 Error	Stg Addr Bus 8-15 Error	Stg Write Bus 0/2 Error	Stg Write Bus 1/3 Error	Stg Addr Bus 1-13	MPL File Not Ready			

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

1. *Match Check 1 register indication with pattern at left. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information*

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ERROR DESCRIPTION	ACTION REQUIRED	FIELD REPLACEABLE UNITS in order of probability of failure			REFERENCE
Stg Addr Bus 1-7 error and Stg Addr Bus 8-15 error	A. Set IAR to '7FFC', '0000', and '0404'. If incorrect parity, picked bits or dropped bits go to card replacement. Otherwise, go to B.	B2T2	B2N2	B2S2	RL205
					RL104
	B. Possible clocking or format decode problem.	B2N2	B2H2	B2T2	RL205
					RL104
	C. If none of the above correct problem, go to FSI section, Fault Symptom Code '34C0', and '34C8'.				
Stg Write Bus 0/2 error	A. If SC register parity incorrect, go to card replacement. Otherwise go to B.	B2D2	B2H2	B1P2	RL303
	B. (1) If SA register parity incorrect, swap B2D2 with B2E2. Rerun test; if SA register still fails, go to C. Otherwise replace card now in B2E2.				
	(2) If SA register parity correct, go to C.				
	C. SA and SC parity correct. Go to card replacement and if failure persists, suspect trilead problem between B2 and control storage board. Trileads for write are shown on FSI 33. If no trilead problem, go to D.	*B2B2			
	D. If none of the above correct problem, go to FSI section, Fault Symptom Code '3420'.				

HARDCORE CHECK 1 ANALYSIS

CHECK 1 REGISTER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
On = Early, Off = Late	Clock Error	CS Decode Error	A Register Parity Error	B Register Parity Error	ALU Check	MPL File Read Check	Stg Addr Bus 1-7 Error	Stg Addr Bus 8-15 Error	Stg Write Bus 0/2 Error	Stg Write Bus 1/3 Error	Stg Addr Bus 1-13	MPL File Not Ready			

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

1. *Match Check 1 register indication with pattern at left. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	ERROR DESCRIPTION	ACTION REQUIRED	FIELD REPLACEABLE UNITS in order of probability of failure			REFERENCE
0	0	0	0	0	0	0		0	0	0	1					Stg Write Bus 1/3 error	A. If SB has incorrect parity, suspect cards listed.	*B2E2	B2J2		RL403
																	B. If SD has incorrect parity, suspect cards listed.	*B2E2	B2L2		
																	C. SB and SD parity correct, suspect cards listed.	*B2C2	B3D2		
																	D. If card replacement does not fix, suspect trileads between B2 and control storage boards. Trileads are shown on FSI 33. Refer to FSI section, Fault Symptom Code '3410'.				
0	0	0	0	0	0	0		0	0	1	1	0	0			Stg Write Bus 0/2 error and Stg Write Bus 1/3 error	A. If SA, SB, SC or/and SD have incorrect parity, suspect cards listed. Refer to FSI section, Fault Symptom Code '3430'.	B1N2	B1P2	B2S2	RL303 RL403
																	B. If SA, SB, SC, and SD have correct parity, suspect cards listed. Refer to FSI section, Fault Symptom Code '3430'.	B3D2		B2B2 B2C2	
0	0	0	0	0	0	0		0	0	0	0	1	0			Stg Addr Bus 1-13 error	Address error detected in control storage. Suspect card(s). If failure persists, suspect trilead or termination problem (refer to FSI 32 check 1 analysis).	B3C2	B3U2		FSI 32
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		MPL file not ready	Refer to FSI section, Fault Symptom Code '3402'.	B2S2	B1S2	B1T4	

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HARDCORE CHECK 1 ANALYSIS

MICRO 166

CHECK 1 REGISTER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
On = Early; Off = Late	Clock Error	CA Decode Even Error	CA Decode Odd Error	CB Decode Even Error	CB Decode Odd Error	Branch/Status Error	Special Operation Error	(Storage) Read 'p' Error 0/2	(Storage) Read 'p' Error 1/3	CU Cycle Error	CD Decode Error				

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

1. *Match Check 1 register indication with pattern at left. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*

ERROR DESCRIPTION	ACTION REQUIRED	FIELD REPLACEABLE UNITS in order of probability of failure	REFERENCE
CA Decode Even error. CA Decode Odd error.	A. If BAR = '0000' or 'FFFF' (1) Swap B1F2, B1M2 (even register decode) with B1E2, B1L2 (odd register decode); set IAR to '0000'; operate Single Instruction switch. (2) If error recurred, failure is either trilead or CA decode card. Refer to logic and scope error output (B2K2, J02 or J05). Verify error, and that only decode of 0 is active while recycling address '0000' in Check Bypass mode. (3) If error moved to opposite decode, (odd to even—even to odd) one of two cards swapped is defective. Swap one at a time to original position to isolate or scope.	B2K2 / Even B1F2* / Even B1M2* / Odd B1E2* / Odd B1L2*	RL207
	B. If BAR = '0004' Either hot 0 decode or decode 12 (TB register) failed. Swap B1M2 and B1L2 with power on. Set IAR to 0004 and operate SI. If failure moves, replace bad card. If failure does not move, refer to logic and scope while recycling address '0004' in Check Bypass mode.	B1M2* / B2K2	RL207
	C. If BAR = '0118' thru '0178' HC01 uses these addresses to test all CA decodes of the register being tested. Using value in BAR, refer to table to determine register and cards involved. Swap register card for decode in error with a like card to try and isolate.	BAR / Register / Register Card / Decode Card 0118 TD, 011C MD, 0128 ND — B1F2* 0130 GC, 0138 TC, 013C MC, 0148 NC — B1L2* 0150 GA, 0158 TA, 0160 MA, 0168 NA — B1E2* 0170 MB, 0174 GB, 0178 NB — B1M2* Decode Card: B2K2	
	D. BAR = any other address or failure is intermittent Using failing word identified by BAR, refer to CAS logic on START 100 and determine failing decode (register being gated to A-bus). See table 1 START 85. Refer to logic and swap register card with common card or if necessary scope while recycling address from BAR in Check Bypass mode. Suspect card contact, trileads, and board land patterns.	B2K2 / B1F2 / B1E2 / B1L2	
CA Decode Even & Odd error.	Replace cards listed.	B2K2 / B2N2	

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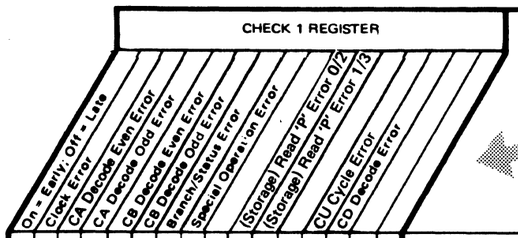
HARDCORE CHECK 1 ANALYSIS MICRO 166

HARDCORE CHECK 1 ANALYSIS



BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

1. *Match Check 1 register indication with pattern at left. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information*

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	ERROR DESCRIPTION
1	0	0	0	1	0				0	0		0	0			CB Decode Even error.
1	0	0	0	0	1				0	0		0	0			CB Decode Odd error.
1	0	0	0	1	1				0	0		0	0			CB Decode Even & Odd error.

ACTION REQUIRED

A. If BAR = '0000' or 'FFFF'

Either a failure to decode CB Decode 16 (0—no register gated to B-bus) or a hot decode is present. Perform the following operations:

(1) Enter/Display switch to Register Select. Operate Reset switch.

(2) Scope **B2J2 S12 (CB even decode error) or B2J2 U11 (CB odd decode error).** Observe the scope for a minus level (plus = failure) while rotating the Register Select switch through its entire range (inner and outer). A failure to decode a register will result in only that register failing (plus level). A hot decode for a register will be indicated by only that register working (minus level). Refer to table for card replacement. If card replacement does not correct problem, suspect trilead.

B. If BAR = See table

This is most probably a failure to properly decode the CB field (register gated to B-bus). If card replacement does not work, suspect trileads.

BAR	Register	Card Replacement Order		
0008	SA	B2D2*	B2F2	B2J2
002C	ST	B2F2	B2E2*	B2J2
0038	BR	B2F2	B2J2	B2D2*
003C	NB	B1M2*	B2J2	
0060	GB	B1M2*	B2J2	
0090	SC	B2F2	B2J2	B2E2
009C	SD	B2E2*	B2F2	B2J2
00A0	SB			
0118	MD	B2F2*	B2J2	
0120	ND			
0128	GC	B1L2*	B2J2	
0130	TC			
0138	MC			
0140	NC			
0148	GA	B1E2*	B2J2	
0150	TA			
0158	MA			
0160	NA	B2E2*	B2J2	
0168	MB	B1M2*	B2J2	
0178	TB			
0184	GD	B1F2*	B2J2	
01F8	TD			
0904	E or F	B2J2		

C. If above symptoms do not apply, refer to CAS logic on START 100 using word displayed from BAR address. Determine register being used and refer to table in step A above for card replacement. If necessary to scope, recycle on test or word that created failure. Refer to FSI section, Fault Symptom Code '3384' or '3388'.

Replace cards listed.

FIELD REPLACEABLE UNITS in order of probability of failure			REFERENCE
			DE504
All CB odd registers fail	B2J2	B2G2	B1G2,B1E2
All CB even registers fail	B2J2	B2G2	B1G2,B1E2
GB, TB, MB, NB,fail	B1M2*	B2J2	B1F2, B2F2
TD, MD, GD, ND fail	B1F2*	B2J2	
SA, SC, BR fail	B2P2	B2F2	B2J2
SB, SD, TG, ST fail	B2E2*	B2F2	B2J2
GA, NA, MA, TA fail	B1E2*	B2J2	
GC, MC, NC, TC fail	B1L2*	B2J2	
No registers fail	B2J2	B2G2	B2Q2,B1P2
GF, TF, NF, MF, fail	B1G2	B2J2	B1F2
GE, TE, NE ME fail	B2J2	B1K2	B1L2
B2J2	B2G2	B2N2	DE504

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HARDCORE CHECK 1 ANALYSIS

CHECK 1 REGISTER

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
On = Early; Off = Late	Clock Error	CA Decode Even Error	CA Decode Odd Error	CB Decode Even Error	CB Decode Odd Error	Branch/Status Odd Error	Special Operation Error	(Storage) Read 'P' Error 0/2	(Storage) Read 'P' Error 1/3	CU Cycle Error	CD Decode Error				

BITS
1 = Must be ON
0 = Must be OFF
BLANK = Ignore

1. *Match Check 1 register indication with pattern at left. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	ERROR DESCRIPTION	ACTION REQUIRED	FIELD REPLACEABLE UNITS in order of probability of failure			REFERENCE
1	0	0	0	0	0	1			0	0		0	0			Branch/Status error	A. With clock stopped and Enter/Display switch in IAR position, turn Address/Data Low switch to value of 3. Observe Register/Storage Display lights for correct parity. If parity is correct, go to B. Otherwise, replace card. If problem still exists, suspect trileads from control storage to B2 board. See FSI 33 for layout of trileads.	B2L2			DE306
																	B. With error condition, display register ST. If incorrect parity, replace card.	B2F2	B2L2		DE306
																	C. If necessary to scope to correct problem, use word at address indicated by BAR and refer to CAS logic on START 100 to decode branching conditions. This enables you to know what should and should not be active in branching circuits. Cycle failing test (HC00-0B recycle addresses listed on MICRO 60 or failing address from BAR.	B2L2	B2F2	B2M4 B1Q2 B2N2 B2Q2	DE306
1	0	0	0	0	0		1		0	0		0	0			Special Operation error.	If card replacement does not correct problem, refer to table below and CAS logic on START 100 with word identified by address from BAR. This enables you to know which Special Op should be active at this time. Special Op format is F; byte 0, bits 2 and 3 identify high order of decode. Byte 1, bits 4-7, identifies low order. See example. If necessary, scope Special Op circuit while recycling address from BAR in Check Bypass mode. Suspect trileads.	B1U4	B2H2	B2L2 B2F2	DE401
1	0											1	0			CU Cycle Error	Replace cards listed. Refer to CTRL 40 for theory and logic on KK301.	B2P2	B2N2		KK301

BAR	Spec Op	Decimal	BAR	Spec Op	Decimal
00AC	'0A'	10	0C38	'05'	5
00FC	'06'	6	0C3C	'08'	8
0718	'0C'	12	0C40	'09'	9
0A04	'0D'	13	0C44	'0F'	15
0AB0	'14'	20	0C48	'10'	16
0AB8	'13'	19	0C64	'11'	17
0AD8	'07'	7	0C68	'16'	22
0B00	'15'	21	0C6C	'17'	23
0B08	'03'	3	0C70	'18'	24
0B74	'0E'	14	0C74	'1A'	26
0BFC	'12'	18	0C7C	'1E'	30
0C24	'01'	1	1F70	'1C'	28
0C28	'04'	4			

Example

binary weight

	32	16		8	4	2	1
Byte 0 bits	2	3	byte 1, bits	4	5	6	7
	0	1		0	1	0	0

Spec Op 20 decode (14 – Hex)

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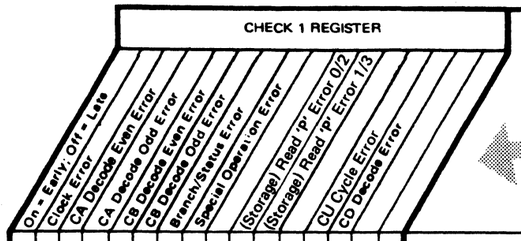
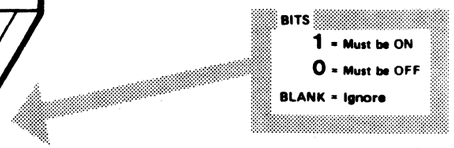
HARDCORE CHECK 1 ANALYSIS





1. ***Match Check 1 register** indication with pattern at left. Take action indicated.*
2. ***Refer to START 900-911 for data flow by card and common card information.***

ERROR DESCRIPTION	ACTION REQUIRED	FIELD REPLACEABLE UNITS in order of probability of failure			REFERENCE
CD Decode error.	A. If BAR = '0000' or '0004' Suspect some decode line hot. CD decode 16 (0 — no register gated to D-bus) should be the only active decode at address '0000' or '0004'. To isolate, perform the following operations. (1) Enter/Display switch to Register Select. (2) Connect a jumper between B1T4 B02 and B2N2 S08. (This allows constant CD set.) Operate Reset. (3) Scope B1P2 U10 (—CD Decode Error) for a plus level as you rotate the Register Select switch through each position of inner and outer ring. (Failing decode is the only one that will be a positive level.) (4) Replace cards as listed. (Do not forget to remove jumper after fix.)	No registers fail (stays minus)	B1P2	B2J2 B2Q2	RC105
		All registers fail (stays plus)	B2J2	B1P2 B2P2	
		SA, SB, SC, SD registers fail	B2S2	B1P2	
		MA register fail	B1D2	B1P2	
		MB register fail	B1Q2	B1P2	
		NA register fail	A1F2	B1P2	
		Any other combination that fails	B1P2 B1S2	B2J2 B2Q2	B2N2 B2P2

B. If BAR = value listed in table, see table. Failure is most likely CD decode of previous word.

BAR=	Register	CD Decode	FRU	External Input	Rd Bus Input	Clock Input to Decode	Check Register
0020	NB	22	B1P2	B1T4	B2J2	B2N2	B2Q2
0030	ST	17		B2K2			
0034	GB	04		B2K2			
0038	ST	17		B2K2			
003C	GB	04		B2K2			
0040 0044	BR	14		B2K2 B2H2			
0078 007C	SD	03		B2S2 B1Q2			
0080 0084	TG	19		B2S2			
00A0 00A4	SA	00		B2S2	B2K2		
00F0	SC	02					
00F8	SC	02					
00F2	SB	01					
011C	MD	12		A1S2 B1D2	B2J2 B2K2		

BAR=	Register	CD Decode	FRU	External Input	Rd Bus Input	Clock Input to Decode	Check Register
0124	ND	20	B1P2	B1U4	B2J2 B2K2	B2N2	B2Q2
012C	GC	13			B2J2 B2K2		
0134	TC	23		B2Q2	B2J2 B2K2		
013C	MC	15		A1S2	B2J2 B2K2		
0144	NC	21		A1S2	B2J2 B2K2		
014C	GA	05			B2J2 B2K2		
0154	TA	09		B2F2	B2J2 B2K2		
015C	MA	11		B1D2 B1U4	B2J2 B2K2		
0164	NA	07		A1F2 B1U4 A1T2	B2J2 B2K2		
016C	MB	08		B1Q2 B1U4	B2J2 B2K2		
017C	TB	06		B2P2	B2J2		
0184	GD	18			B2K2		
01F8	TD	10		B2P2	B2K2		

*Multiple usage card

Continued on next page.

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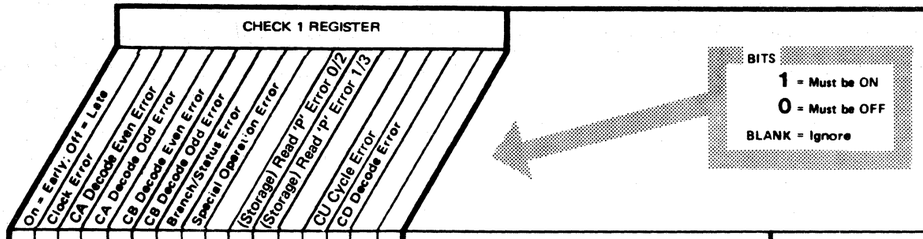
HARDCORE CHECK 1 ANALYSIS



1. *Match Check 1 register indication with pattern at left. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	ERROR DESCRIPTION	ACTION REQUIRED	FIELD REPLACEABLE UNITS in order of probability of failure			REFERENCE
																CD Decode error (continued)	C. If above symptoms do not apply, recycle test showing failure. Refer to START 100 with word displayed by stopping on address of word preceding BAR address and determine correct CD decode (register that should have been destined). Scope input to CD decode error circuit to determine decode that is activating erroneously. Refer to FSI section, Fault Symptom Code '3204'. *Note: If failure is occurring often enough, the procedure in A above may be of use here also.*				RC105
1	0								1	0						(Storage) Read 'P' Error 0/2	Go to FSI 32 and determine failing unit.		1–B3T2	2–B3C2	FSI 32
																		3–B3F2	4–B3G2	5–B3H2	
																		6–B3J2	7–B3K2	8–B3L2	
																		9–B3D2			
1	0								0	1						(Storage) Read 'P' Error 1/3					
1	0								1	1						(Storage) Read 'P' Error 0/2 and or 1/3					
1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0			B2N2			

*Multiple usage card

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CHANNEL WRAPAROUND TEST

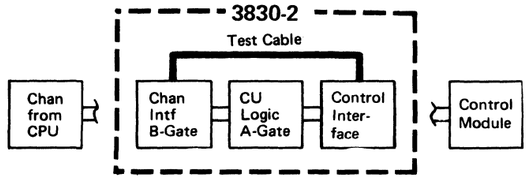
BRIEF DESCRIPTION

To verify that the channel interface logic in the 3830-2 is functioning properly, a test cable and a microdiagnostic are provided.

The microdiagnostic cannot function without the test cable.

The hardware tested by the diagnostic includes:

1. All channel interface (CHL-I) line drivers and receivers except Clock Out, Metering Out, and Metering In.
2. All logic on the A-A1 board and B-A1 board.
3. The logic associated with channel branch condition; for example, COMMO, SUPPO.
4. The logic associated with channel interface Check 2 errors.
5. The channel I/O receptacles, wires to the B-gate, and wires to the A-gate are all tested because the test cable replaces the channel serpent connectors.



CABLE INSTALLATION INSTRUCTIONS

The following instructions and diagrams are based on the assumption that the 3830-2 has the Two Channel Switch Additional feature. If the 3830-2 does not have the Two Channel Switch Additional feature, disregard references to channels C and D. If the 3830-2 does not have the Two Channel Switch feature, disregard references to channel B also.

1. Set the channel A, B, C, and D Enable/Disable switches (on the 3830-2 power sequence panel) to Disable and wait for the Disabled lamp (CE panel) to come on.
2. Disconnect the channel bus and tag cables at the 3830-2 for the channel(s) to be tested.

   Note: If the customer desires to have the processor available, terminate or butt the cables just removed.

3. Install the test cable (P/N 2346603) by plugging one end into the channel interface tag in and bus in connectors and the other end into the control interface connectors.

   Diagnostics may be run on two channels at one time: A and B, or C and D. (No other combination may be used.)

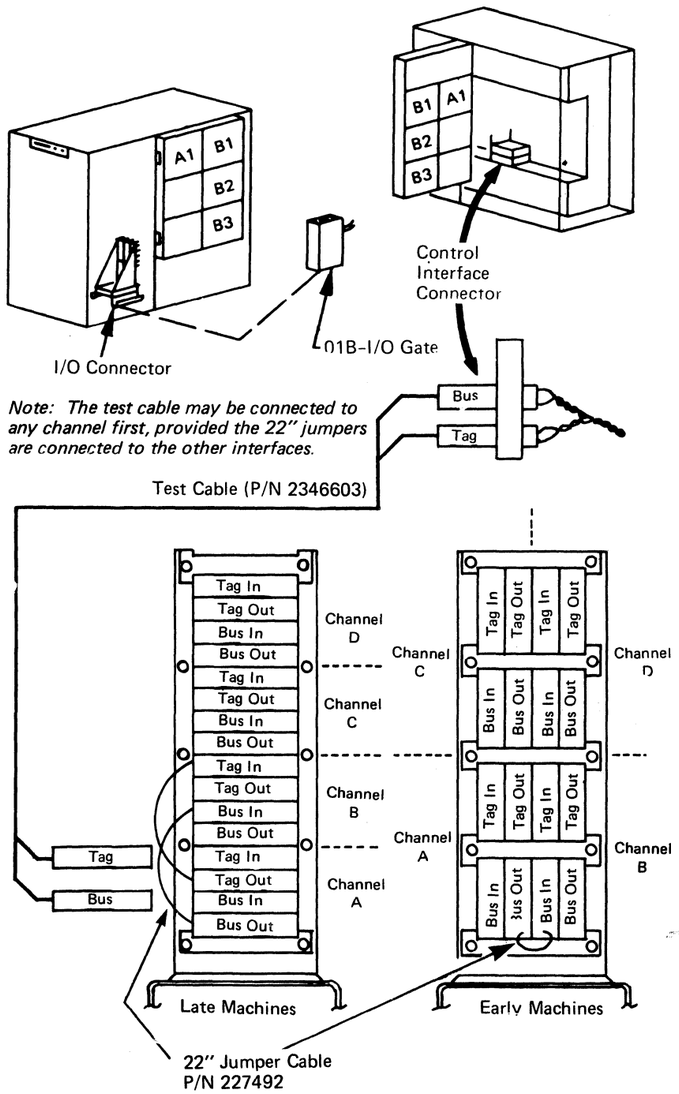
   For two channel testing, use jumper cables (P/N 2227492), as shown, to couple channels. Terminate last channel being tested by using tag terminator (P/N 5440650 or 2282676) and bus terminator (P/N 5440649 or 2282675).

   For single channel testing, jumper cables are not needed, but the channel being tested must be terminated.

4. Run microdiagnostic routines 60 thru 6E.

SERVICE HINT: Channel Interface Wiring Checkout

After running channel wraparound test in the usual manner, recable I/O connectors in reverse order and repeat the test. For example, if cables were connected A to B with B terminated, then reverse cables (B to A with A terminated). Test only the terminated channel. If errors occur, suspect exit wiring or connectors on the unterminated channel. Repeat procedure for interfaces C and D if applicable.

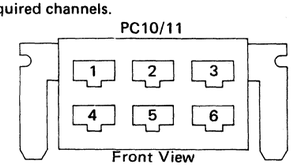


Note: The test cable may be connected to any channel first, provided the 22" jumpers are connected to the other interfaces.

Figure 1: Remote Switch Enabling

If Remote Switch feature is installed but not connected, jumper the indicated pins to enable the required channels.

Ch. A. — PC10-1 to PC10-2
Ch. B. — PC10-4 to PC10-5
Ch. C. — PC11-1 to PC11-2
Ch. D. — PC11-4 to PC11-5



MICRODIAGNOSTIC RUNNING INSTRUCTIONS

1. Verify that Channel A, B, C, and D Enable/Disable switches are set to Disable and that the Channel Interface Disabled lamp is on.
2. Connect wraparound cable. (See "Cable Installation Instructions", this page.)
3. If two interfaces are being tested simultaneously, check that they do not have the same CU address. If they do, one must be altered.
4. IMPL if necessary (see START 25, entry A through normal completion, display "C484").
5. Set Operation Mode switch to Forced Logging and set Enter/Display Switch to Program Data Entry/Display.
6. Set Data Entry switches to "60" and operate Execute switch. (Tests must always be started by running routine 60 first.)
7. Set Data Entry switches to "38" and operate Execute switch. This causes an error display of "8102" or "8103". This error must be forced to successfully execute routines 60 through 6E.
8. Enable the desired channel interfaces. Not more than two interfaces can be tested at one time: A and B, or C and D. All interfaces not being tested must be disabled. If remote switch feature is installed but not connected see Fig. 1.
9. Set Data Entry switches to 60 and operate Execute sw.
10. Turn on Multitag switch if interfaces A and B, or interfaces C and D are to be tested as a pair. Turn off Multitag sw. for individual testing of interfaces.
11. Enter parameters as follows: Set Data Entry switches to 10 and operate Execute sw. Then set Data Entry switches according to the following:

    00 — Test both interfaces A and B
    20 — Test interface A only (or single channel)
    21 — Test interface B only
    02 — Test interfaces C and D
    22 — Test interface C only
    23 — Test interface D only

    Operate Execute sw. Then set Data Entry switches to:

    00 — All tests

    Operate Execute switch. Then set Data Entry Switches to:

    00-16 Drive Addresses (Standard Machine)
    01-32 Drive Addresses (32 Drive Expansion)
    00-8 Drive Addresses (bit 2 off or on)
    08-16 Drive Addresses (bit 2 off or on)
    10-16 Drive Addresses (Bit 3 floating)
    20-16 Drive Addresses (bit 2 floating)
    18-32 Drive Addresses (bit 2 off or on)
    28-32 Drive Addresses (bit 2 floating)
    30-32 Drive Addresses (Bit 2 and 3 floating)
    38-64 Drive Addresses

    } See Note 1

    Operate Execute switch to start tests.
12. Routines 60-6E will run until normal completion (Clock Stopped and Check 2 lamps on) or until an error is detected (message 81xx). If an error does occur, refer to MICRO 25.

    The normal stops are defined by a clock stopped condition, with the content of IAR defining the correct stop of the program looping with a dynamic IAR address defining the correct stop. The normal stops and the CE actions are shown in the table at the right.

    Note: *To rerun tests on the same channel(s), only steps 8 through 11 need be performed.*
13. Restore cables, etc., to normal and perform IMPL with the functional microprogram disk.

    Note 1: For 3344 or 3350 Attachment Features. Refer to label on address card for parameter.

CE PANEL INDICATIONS	CE ACTION
Clock Stopped and Check 2 lamps on	1. Momentarily turn the Enter/Display switch to IAR and verify that the address is '0040'. Enter/Display switch must be returned to Program Data Entry/Display position before program will continue. 2. Turn Operation Mode switch to CE Normal. Clock will start and program will loop.
Program looping and Check 2 lamp on	1. Turn Operation Mode switch to Forced Logging. 2. Operate Execute switch.
Clock Stopped and Check 1 lamps on	1. Turn Operation Mode switch to CE Normal. 2. Operate Start switch. Clock will start and program will loop.
Program looping	1. Turn Operation Mode switch to Forced Logging. 2. Operate Execute switch.
Clock Stopped and Check 2 lamps on	1. Momentarily turn the Enter/Display switch to IAR and verify that the address is '0040'. Enter/Display switch must be returned to Program Data Entry/Display position before program will continue. 2. Turn Operation Mode switch to CE Normal. Clock will start and program will loop.
Program looping and Check 2 lamp on	1. Turn Operation Mode switch to Forced Logging. 2. Operate Execute switch.
On two or four channel switch machine, the Program Display lamps will ripple until the Multitag switch is turned off. If the lamps fail to ripple, the Multitag switch is failing.	Turn off Multitag switch.
If two interfaces are being tested, the program will return to beginning of this table and repeat the entire procedure (for interface B or D). If one interface is being tested or if this is the second time through the procedure, a normal completion message (C'46E') should be displayed. End of Test.	

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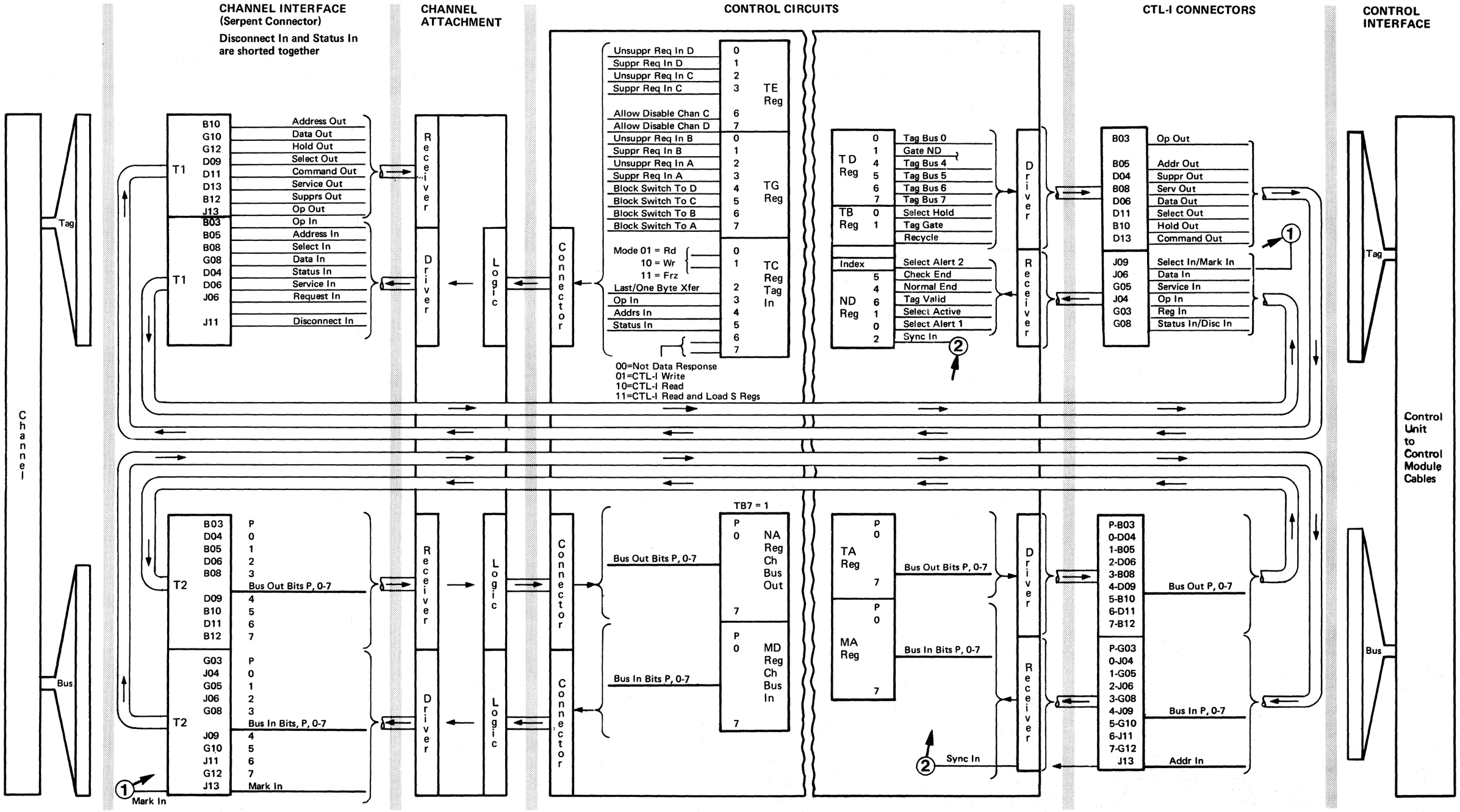

3830-2

AU3200 Seq 2 of 2	2347030 Part No. (8)

See E/C History	447461 12 Mar 76	447465 15 Dec 78				

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60-6E CHANNEL WRAPAROUND TESTS (Part 1 of 2)

Microdiagnostic Routines	Operating Mode			Control Options (MICRO 16)	Parameter Entries			Comments
	STAND-ALONE	INLINE	ONLINE		BYTE NO.	DEFAULT VALUE	RANGE AVAILABLE	
60 Alters certain words in the control microprogram, and tests for correct operation of system reset. For intermittent failures, run under loop option 32. See MICRO 17 for description of routines linked and operating restrictions.	Yes	No	No	02 3A 01 3E 32	1	00	**Interface(s) Tested** 00 – A and B 20 – A only 21 – B only 02 – C and D 22 – C only 23 – D only	Operating Procedures: 1. Set Operation Mode switch to Forced Logging position. 2. Set Enable/Disable switch(es) to Disable. (If more than one interface is to be tested, both addresses cannot be the same; refer to INST 20.) 3. Load and execute routine 60. The program should stop with error display '8102' (or '8103' if interface tested is B or D only). 4. Set Enable/Disable switch(es) to Enable on only those interfaces to be tested. Turn on Multitag switch if more than one interface is to be tested.) 5. Load and execute the desired routine 60 – 6E. The routine will execute and link up through routine 6E, or until an error occurs. Note 2. To run only one test of a routine* do steps 1 – 4 of above procedure, then: 1. Load desired routine 60, 62, 64, 6C, or 6E. 2. Enter '3A' control option (loop on first error). 3. Enter '10' (parameter entry desired). 4. Enter 'XX' (XX = test number to be looped). All tests in the routine will be run until the requested test is run. The requested test will then loop until stopped by the CE. **Use the MICFL section for information on test numbers and routine operation.* *Note 1:* 00-16 Drive Addresses (Standard Machine) 01-32 Drive Addresses (32 Drive Expansion) 00-8 Drive Addresses (bit 2 off or on) 08-16 Drive Addresses (bit 2 off or on) 10-16 Drive Addresses (Bit 3 floating) 20-16 Drive Addresses (bit 2 floating) 18-32 Drive Addresses (bit 2 off or on) 28-32 Drive Addresses (bit 2 floating) 30-32 Drive Addresses (Bit 2 and 3 floating) 38-64 Drive Addresses } For 3344 or 3350 attachment features, refer to label on address card for parameter. *Note 2:* *If a check 1 error occurs, other than in routine '6E', record IAR, BAR Check 1 register contents and go to FSI.*
					2	00	00 – All tests F8 – System Reset Tests F4 – Selective Reset Test	
					3	00	**Features** See Note 1	
62 Tests for: Active bus in or bus out lines. Active in tags. Active channel branch conditions.	Yes	No	No	02 3A 01 3E 32	1	00 All Tests	**Test No.** From byte 2 of error bytes. (See MICRO 225 – 265.)	
64 Tests for: Suppressible and nonsuppressible Request In. Bus out data path. Bus in data path.								
66 Tests for: Initial Selection sequence. Halt I/O	Yes	No	No	02 3A 01 3E 32	None	–	None	
68 Tests for: Nonselection when an incorrect unit address is presented.	Yes	No	No	02 3A 01 3E 32	1	00 All Addresses	A single control unit address to be tested	
6A Tests for: Short busy sequence. Two Channel Switch.	Yes	No	No	02 3A 01 3E 32	None	–	None	
6C Tests for: Correct data transfer with Read command. Correct data transfer with Write command. Read truncation. Halt I/O during read. Write overrun. One byte write.	Yes	No	No	02 3A 01 3E 32	1	00 All Tests	**Test No.** From byte 2 of error bytes. (See MICRO 320 – 335.)	

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60-6E CHANNEL WRAPAROUND TESTS (Part 2 of 2)

Microdiagnostic Routines	Operating Mode			Control Options (MICRO 16)	Parameter Entries			Comments
	STAND-ALONE	INLINE	ONLINE		BYTE NO.	DEFAULT VALUE	RANGE AVAILABLE	
6E Tests for: 1. Disconnect In sequence 2. Selective Reset	Yes	No	No	02 3A 01 3E	1	All Tests	FC——Selective Reset test F8——Disconnect In test	Turn on Multitag switch (machines with Two Channel Switch or Two Channel Switch Additional). Turn Operation Mode switch to Forced Logging position. **CE PANEL INDICATIONS** / **CE ACTION** 1. Clock Stopped and Check 2 lamp on — 1. Momentarily turn the Enter/Display switch to IAR and verify that the address is '0040'. Enter/Display switch must be returned to Program Data Entry/Display position before program will continue. Turn Operation Mode switch to CE Normal; Clock will start and program will loop 2. Program is looping and Check 2 lamp on — 2. Turn Operation Mode switch to Forced Logging. Operate Execute switch. 3. Clock Stopped on and Check 1 lamp on — 3. Turn Operation Mode switch to CE Normal. Operate Start switch. Clock starts and program loops. 4. Program is looping — 4. Turn Operation Mode switch to Forced Logging. Operate Execute switch 5. Clock Stopped and Check 2 lamp on — 5. Momentarily turn the Enter/Display switch to IAR and verify that the address is '0040'. Enter/Display switch must be returned to Program Data Entry/Display position before program will continue. Turn Operation Mode switch to CE Normal Clock will start and program will loop. 6. Program is looping and Check 2 lamp on — 6. Turn Operation Mode switch to Forced Logging. Operate Execute switch. 7. On machines with Two Channel Switch or Two Channel Switch Additional, the Program Display lamps will ripple until the Multitag switch is turned off. If lamps fail to ripple, the Multitag switch is failing. — 7. Turn off the Multitag switch. 8. If two interfaces are being tested, and Multitag switch is in the off position, program display will be blank. However the program will return to step 1 above, and repeat the entire procedure (for interface B). If one interface is being tested or if this is the second time through the procedure, a normal completion message 'C46E' should be displayed. End of test. 9. Restore cables, etc. to normal and perform an IMPL operation with the functional microprogram disk.

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 60)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6002		Not Used	Not Used	A-A1Q2 *A-A1M2 *B-A1C2 A-A1R2 A-A1L2 A-B2M2	A-B2M2 *A-A1M2 A-A1L2 A-A1R2 A-B2S2 A-A1S2 A-B2P2 A-B2Q2	*A-A1Q2 *A-A1M2 *B-A1C2 A-A1R2 A-A1L2	*A-A1P2 *A-A1M2 *B-A1C4 A-A1R2 A-A1L2 A-B1R2 A-B1U4	*A-A1K2 *A-A1M2 *A-A1H2 A-A1R2 A-A1L2	*A-A1J2 *A-A1M2 *A-A1H4 A-A1R2 A-A1L2	0540	**SYSTEM RESET FAILED TO OCCUR (CHAN A AND B, C AND D, A ONLY OR C ONLY)** This is a normal stop the first time through the routine. See MICRO 200 Note 2, and MICRO 210 routine summary. This error occurs if: a. The Enable/Disable switch for channel A or B is in the Disable position while trying to run channel A and B or A only. b. A problem exists in the System Reset circuitry. c. The Channel Wrap Cable is connected incorrectly.	Refer to System Reset and Selective Reset CHL-I 190
6003		Not Used	Not Used								**SYSTEM RESET FAILED TO OCCUR (CHAN B OR D)** This error occurs if: a. The Enable/Disable switch for channel B is in the Disable position while trying to run channel B only. b. A problem exists in the System Reset circuitry for channel B. c. The Channel Wrap Cable is connected incorrectly.	Refer to System Reset and Selective Reset CHL-I 190
6006		Not Used	Not Used			*A-A1Q2 *A-A1M2 *B-A1C2 A-A1R2 A-B2M2		*A-A1K2 *A-A1M2 *A-A1H2 A-A1R2 A-B2M2		0580	**SYSTEM RESET WORKED FOR B (D) AND FAILED FOR A (C)** This error may occur if: a. The Enable/Disable switch is in the Disable position while trying to run channel B or D only. b. A problem exists in the System Reset circuitry.	Refer to System Reset and Selective Reset CHL-I 190
6007		Not Used	Not Used				*A-A1P2 *B-A1C4 A-A1R2 *A-A1M2 A-B2M2		*A-A1J2 *A-A1H4 A-A1R2 *A-A1M2 A-B2M2	0580	**SYSTEM RESET WORKED FOR A (C) AND FAILED FOR B (D)** This error may occur if: a. The Enable/Disable switch is in the Disable position while trying to run channel A and B, A only, C and D, or C only. b. A problem exists in the System Reset circuitry.	Refer to System Reset and Selective Reset CHL-I 190
6008		Not Used	Not Used				A-A1R2 A-B1U4		A-A1R2	0430	**SYSTEM RESET- CHANNEL A (C) WHILE RUNNING CHANNEL B (D)** A System Reset occurred in channel A (C)	Refer to System Reset and Selective Reset CHL-I 190

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 60)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6009		Not Used	Not Used	A-A1R2 A-B1R2		A-A1R2		A-A1R2		0430	**SYSTEM RESET - CHANNEL B (D) WHILE RUNNING CHANNEL A (C)** A System Reset occurred in Channel B (D).	Refer to System Reset and Selective Reset CHL-I 190
6010 **6011**		Not Used	Not Used	A-A1Q2 *B-A1C2		*A-A1Q2 *B-A1C2	*A-A1P2 *B-A1C4	*A-A1K2 *A-A1H2	*A-A1J2 *A-A1H4	0430	**A SELECTIVE RESET WAS PERFORMED WHILE THE CU WAS NOT SELECTED** This resulted in a System Reset. Suppress Out evidently failed.	Refer to System Reset and Selective Reset CHL-I 190
600A		Not Used	Not Used			*A-A1Q2 *B-A1C2		*A-A1K2 *A-A1H2		0540	**TWO RESETS OCCURRED WHILE RUNNING CHAN A (C) ONLY** Only one System Reset should occur when running options for only one channel. If this error occurred as a result of changing options (for example, from A to B, or from A and B to A), a re-IMPL may be necessary.	Refer to System Reset and Selective Reset CHL-I 190
600B		Not Used	Not Used				*A-A1P2 *B-A1C4		*A-A1J2 *A-A1H2	0540	**TWO RESETS OCCURRED WHILE RUNNING CHANNEL B (D) ONLY** Only one System Reset should occur when running options for only one channel. If this error occurred as a result of changing options (for example, from A to B, or from A and B to A), a re-IMPL may be necessary.	Refer to System Reset and Selective Reset CHL-I 190
600E **600F**		Not Used	Not Used	A-A1Q2 *A-A1M2 A-B2P2	A-B2P2 *A-A1M2	*A-A1Q2 *A-A1M2	*A-A1P2 *A-A1M2	*A-A1K2 *A-A1M2	*A-A1J2 *A-A1M2	0540	**SELECTIVE RESET OCCURRED WITH NO SELECTION (CHAN A, B, C, OR D)** A Selective Reset was initiated to a machine that was not selected. This should have resulted in no Selective Reset. A test revealed that a Selective Reset had taken place.	Refer to System Reset and Selective Reset CHL-I 190

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 62)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6204 6205		Not Used	Not Used	*B-A1C2	*B-A1C2 *B-A1C4 *A-A1H2 *A-A1H4					0434	**DATA IN BIT IS ON** The In Tags were gated to a register and tested. When sampled, the Data In bit was found to be on.	Refer to CHL-I 35
6208 6209		Not Used	Not Used	*B-A1C2	*B-A1C2 *B-A1C4 *A-A1H2 *A-A1H4		A-B2S2			0434	**SERVICE IN BIT IS ON** The In Tags were gated to a register and tested. When sampled, the Service In bit was found to be on.	Refer to CHL-I 35
620C 620D		Not Used	Not Used	A-A1Q2 *B-A1C2	*B-A1C2 *B-A1C4 *A-A1H2 *A-A1H4	*A-A1Q2 *B-A1C2	*A-A1P2 *B-A1C4	*A-A1K2 *A-A1H2	*A-A1J2 *A-A1H4	044C	**OPERATIONAL IN BIT IS ON** The In Tags were gated to a register and tested. When sampled, the Operational In bit was found to be on.	Refer to CHL-I 220
6210 6211		Not Used	Not Used	A-A1Q2 *B-A1C2 *A-B1L2 A-B2S2	*B-A1C2 *B-A1C4 *A-A1H2 *A-A1H4 *A-B1L2	*A-A1Q2 *B-A1C2 *A-B1L2 A-A1S2 A-B2S2 A-B1T4	*A-A1P2 *B-A1C4 *A-B1L2 A-A1S2 A-B1T4	*A-A1K2 *A-A1H2 *A-B1L2	*A-A1J2 *A-A1H4 *A-B1L2	0434	**REQUEST IN BIT IS ON** The In Tags were gated to a register and tested. When sampled, the Request In bit was found to be on.	Refer to CHL-I 135
6214 6215		Not Used	Not Used	A-A1Q2 *B-A1C2	*B-A1C2 *B-A1C4 *A-A1H2 *A-A1H4	*A-A1Q2 *B-A1C2	*A-A1P2 *B-A1C4	*A-A1K2 *A-A1H2	*A-A1J2 *A-A1H4	0434	**STATUS IN OR DISCONNECT IN BIT IS ON** The In Tags were gated to a register and tested. When sampled, the Status In or Disconnect In bit was found to be on.	Refer to CHL-I 220 for Status In and to CHL-I 130 for Disconnect In
6218 6219		Not Used	Not Used	*B-A1C2	*B-A1C2 *B-A1C4 *A-A1H2 *A-A1H4					0434	**ADDRESS IN BIT IS ON** The In Tags were gated to a register and tested. When sampled, the Address In bit was found to be on.	Refer to CHL-I 220
621C 621D		Not Used	Not Used	A-A1Q2 *B-A1E6 *B-A1D2 *B-A1F2	*B-A1E6 *B-A1F6 *A-A1D2 *A-A1D4 *B-A1D2 *B-A1D4 *A-A1G2 *A-A1G4	*A-A1Q2 *B-A1E6 *B-A1D2 *B-A1F2	*A-A1P2 *B-A1F6 *B-A1D4 *B-A1F4	*A-A1K2 *A-A1D2 *A-A1G2 *A-A1E2	*A-A1J2 *A-A1D4 *A-A1G4 *A-A1E4	0434	**SELECT IN OR MARK IN BIT IS ON** The In Tags were gated to a register and tested. When sampled, the Select In or Mark In bit was found to be on.	Refer to AA401 (channel A), BA401 (channel B), CA401 (channel C), or DA401 (channel D) for Mark In. Refer to CHL-I 220 for Select In

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**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 62)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6220 **6221**		Not Used	Not Used		A-A1S2 A-B2L2					0470	**BOPAR BRANCH IS ON** The BOPAR (Bus Out Parity Check) branch should be off at initial check time. When sampled, it was found active. This error is not channel-dependent.	Refer to CHL-I 165
6224 **6225**		Not Used	Not Used		*A-A1M2 A-B2L2 A-B1Q2					0480	**SELTD BRANCH IS ON** The SELTD (Selected) branch should be off at initial check time. When sampled, it was found active. This error is not channel-dependent.	Refer to CHL-I 220
6228 **6229**		Not Used	Not Used		A-A1U2 *A-A1M2 A-B2L2 A-B1Q2					0500	**ADDRO BRANCH IS ON** The ADDRO (Address Out) branch should be off at initial check time, but when sampled, it was found active. This error is not channel-dependent.	Refer to CHL-I 220
622C **622D**		Not Used	Not Used		*A-A1Q2 *A-A1M2 A-A1U2 A-B2L2 A-B1L2		A-A1R2		A-A1R2	0510	**CUEND BRANCH FOR CHANNEL A (C) IS ON** The CUEND (Control Unit End) branch for channel A (C) should be off at initial check time. When sampled, it was found active.	Refer to CHL-I 145
6230 **6231**		Not Used	Not Used		*A-A1M2 A-B2L2					0508	**COMMO BRANCH IS ON** The COMMO (Command Out) branch should be off during the initial check. When it was sampled, it was found active. This error is not channel-dependent.	Refer to CHL-I 220
6234 **6235**		Not Used	Not Used		*A-A1P2 *A-A1M2 A-A1U2	A-A1R2 *A-A1Q2 A-B1M2 *A-A1M2		A-A1R2		0514	**CUEND BRANCH FOR CHANNEL B (D) IS ON** The CUEND (Control Unit End) branch for channel B (D) should be off at initial check time. When sampled, it was found active.	Refer to CHL-I 145
6238 **6239**		Not Used	Not Used		A-A1R2 A-B1R2					0520	**CHANNEL B (D) BRANCH IS ON** No attempts have been made to select either channel. The machine should be in neutral status (not switched to A (C) or B (D)), and the channel B (D) branch should be off.	Refer to CHL-I 180

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 62)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
623C 623D		Not Used	Not Used		*A-A1M2 A-A1R2 A-B2L2					04F4	**SUPPO BRANCH IS ON** The SUPPO (Suppress Out) branch should be off during the initial check. When sampled, it was found active. This is not channel-dependent.	Refer to CHL-I 150
6240 6241		Not Used	Not Used		A-A1T2 A-A1S2 *A-A1Q2 *A-A1P2 *A-A1K2 *A-A1J2 A-A1N2 A-B2Q2					0484	**CHECK 2 BRANCH IS ON** The Check 2 branch should be off during the initial check. When sampled, it was found active. This error is not channel-dependent.	Refer to PANEL 50. Although A-A1Q2, A-A1P2, A-A1K3 and A-A1J2 cards are alike, they should not be swapped for this error because the same symptom would occur.
6244 6245		Not Used	Not Used		A-A1S2 A-B2L2					0530	**SERVO BRANCH IS ON** The SERVO (Service Out) branch should be off at initial check time. When sampled, it was found active. This error is not channel-dependent.	Refer to CHL-I 220
6248 6249		Not Used	Not Used		A-A1U2 *A-A1M2 A-B2L2					0540	**HLTIO BRANCH IS ON** The HLTIO (Halt I/O) branch should be off during the initial check. When sampled, it was found active.	Refer to CHL-I 140
624C 624D		Not Used	Not Used		A-A1U2 *A-A1M2 *A-A1K2					0548	**CUEND BRANCH FOR CHANNEL C IS ON** The CUEND (Control Unit End) branch for channel C should be off at initial check time. When sampled, it was found active.	Refer to CHL-I 145
6250 6251		Not Used	Not Used		A-A1U2 *A-A1M2 *A-A1J2					0550	**CUEND BRANCH FOR CHANNEL D IS ON** The CUEND (Control Unit End) branch for channel D should be off at initial check time. When sampled, it was found active.	Refer to CHL-I 145

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 62)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6254 **6255**		Not Used	Not Used		A-A1R2 A-B2L2					0558	**X CHANNEL (CHANNEL C/D) BRANCH IS ON** The X channel branch should be off at initial check time. When sampled, it was found active.	Refer to CS104 and CHL-I 150
6284 **6285**		Not Used	Not Used	*B-A1C2 A-A1U2 *A-B1L2	A-A1U2 *A-B1L2	*B-A1C2	*B-A1C4	*A-A1H2	*A-A1H4	22FC	**DATA IN BIT IS ON** After selection, the In Tags were gated to a register and tested. When sampled, the Data In bit was found to be on.	Refer to CHL-I 135
6288 **6289**		Not Used	Not Used	*B-A1C2 A-A1U2 *A-B1L2	A-A1U2 *A-B1L2	*B-A1C2	*B-A1C4	*A-A1H2	*A-A1H4	22FC	**SERVICE IN BIT IS ON** After selection, the In Tags were gated to a register and tested. When sampled, the Service In bit was found to be on.	Refer to CHL-I 135
6290 **6291**		Not Used	Not Used	A-A1Q2 *A-B2F2		*A-A1Q2 *A-B2F2	*A-A1P2 *A-B2F2	*A-A1K2 *A-B1K2	*A-A1J2 *A-B1K2	22FC	**REQUEST IN BIT IS ON** After selection, the In Tags were gated to a register and tested. When sampled, the Request In bit was found to be on.	Refer to CHL-I 135
6294 **6295**		Not Used	Not Used	A-A1Q2 A-B1L2 *B-A1D2 A-A1S2 A-A1R2	*A-B1L2 A-A1S2 A-A1R2	*A-A1Q2 *B-A1D2 A-A1R2	*A-A1P2 *B-A1D4 A-A1R2	*A-A1K2 *A-A1G2 A-A1R2	*A-A1J2 *A-A1G4 A-A1R2	22FC	**STATUS IN OR DISCONNECT IN BIT IS ON** After selection, the In Tags were gated to a register and tested. When sampled, the Status In or Disconnect In bit was found to be on.	Refer to CHL-I 220
6298 **6299**		Not Used	Not Used	*B-A1C2 A-A1Q2 A-A1S2 *A-B1L2	A-A1S2 *A-B1L2	*B-A1C2 *A-A1Q2	*B-A1C4 *A-A1P2	*A-A1H2 *A-A1K2	*A-A1H4 *A-A1J2	22FC	**ADDRESS IN BIT IS ON** After selection, the In Tags were gated to a register and tested. When sampled, the Address In bit was found to be on.	Refer to CHL-I 220
62A0 **62A1**		Not Used	Not Used	A-A1Q2 *A-A1M2 A-A1S2 A-B2L2	*A-A1M2 A-A1S2 A-B2L2	*A-A1Q2 *A-A1M2 *B-A1E2 *B-A1F2	*A-A1P2 *A-A1M2 *B-A1E4 *B-A1F4	*A-A1K2 *A-A1M2 *A-A1F2 *A-A1E2	*A-A1J2 *A-A1M2 *A-A1F4 *A-A1E4	22F8	**BOPAR BRANCH IS ON** The BOPAR (Bus Out Parity Check) branch should be off at initial check time after selection. When sampled, it was found active.	Refer to CHL-I 165

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 62)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
62A8 **62A9**		Not Used	Not Used	A-A1Q2 *B-A1C2		*A-A1Q2 *B-A1C2 *A-A1M2	*A-A1P2 *B-A1C4 *A-A1M2	*A-A1K2 *A-A1H2	*A-A1J2 *A-A1H4	22A4	**ADDRO BRANCH IS ON** The ADDRO (Address Out) branch should be off at initial check time, after selection. When sampled, it was found active.	Refer to CHL-I 220
62AC **62AD**		Not Used	Not Used	A-A1Q2		*A-A1Q2				22B0	**CUEND BRANCH CHANNEL A IS ON** The CUEND (Control Unit End) branch for channel A should be off at initial check time, after selection. When sampled, it was found active.	Refer to CHL-I 145
62B0 **62B1**		Not Used	Not Used	A-A1Q2 B-A1C2 A-A1U2 A-A1S2		*A-A1Q2 *A-A1M2 *B-A1C2	*A-A1P2 *A-A1M2 *B-A1C4	*A-A1K2 *A-A1M2 *A-A1H2	*A-A1J2 *A-A1M2 *A-A1H2	22A8	**COMMO BRANCH IS ON** The COMMO (Command Out) branch should be off during the initial check, after selection. When sampled it was found active.	Refer to CHL-I 220
62B4 **62B5**		Not Used	Not Used				*A-A1P2			22B4	**CUEND BRANCH CHANNEL B IS ON** The CUEND (Control Unit End) branch for channel B should be off at initial check time, after selection. When sampled, it was found active.	Refer to CHL-I 145
62BC **62BD**		Not Used	Not Used	A-A1Q2 *A-A1C2 *A-A1M2		*A-A1Q2 *B-A1C2 *A-A1M2	*A-A1P2 *B-A1C4 *A-A1M2	*A-A1K2 *A-A1H2 *A-A1M2 A-A1R2	*A-A1J2 *A-A1H4 *A-A1M2 A-A1R2	2258	**SUPPO BRANCH IS ON** The SUPPO (Suppress Out) branch should be off during initial check, after selection. When sampled, it was found active.	Refer to CHL-I 150
62C0 **62C1**		Not Used	Not Used	A1Q2	A1S2 B1R2 B1F2	A1R2 A1Q2 A1N2 A1M2 A1L2	A1R2 A1P2 A1N2 A1M2 A1L2	A1K2 A1L2 A1R2	A1J2 A1L2 A1R2	2294	**UNEXPECTED CHECK-2 ERROR** A check-2 error occurred when CU selected.	
62C4 **62C5**		Not Used	Not Used	*B-A1E2 A-A1S2 *A-A1M2	A-A1S2 *A-A1M2	*B-A1E2 *A-A1M2	*B-A1E4 *A-A1M2	*A-A1F2 *A-A1M2	*A-A1F4 *A-A1M2	2294	**SERVO BRANCH IS ON** The SERVO (Service Out) branch should be off during initial check, after selection. When sampled, it was found active.	Refer to CHL-I 180
62C8 **62C9**		Not Used	Not Used	A-A1Q2 *A-A1M2		*A-A1Q2 *A-A1M2	*A-A1P2 *A-A1M2	*A-A1K2 *A-A1M2	*A-A1J2 *A-A1M2	22C8	**HLTIO BRANCH IS ON** The HLTIO (Halt I/O) branch should be off during initial check, after selection. When sampled, it was found active.	Refer to CHL-I 140

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 62)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code ❶	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
62CC **62CD**		Not Used	Not Used					*A-A1K2		22D0	**CUEND BRANCH CHANNEL C IS ON** The CUEND (Control Unit End) branch should be off during initial check, after selection. When sampled, it was found active.	Refer to CHL-I 145
62D0 **62D1**		Not Used	Not Used						*A-A1J2	22D8	**CUEND BRANCH CHANNEL D IS ON** The CUEND (Control Unit End) branch should be off during initial check, after selection. When sampled, it was found active.	Refer to CHL-I 145
62D4 **62D5**		Not Used	Not Used	*B-A1D2 *B-A1E6 A-A1Q2	Connect channel wrap cable to only one channel at a time to isolate the failing channel	*B-A1D2 *B-A1E6 *A-A1Q2 *B-A1C2	*B-A1D4 *B-A1F6 *A-A1P2	*A-A1G2 *A-A1D2 *A-A1K2	*A-A1G4 *A-A1D4 *A-A1J2	04C0	**SELECT IN IS DOWN** 1. This is a propagate test. Select In is gated to a register and tested. When sampled it was found down. 2. Channel wrap cable may be reversed. Check MICRO 200 for proper connections. 3. This error can occur if terminators are swapped or not installed.	This failure will vary depending on priority jumpering and channel interface jumper cabling. Connect to only one channel at a time to isolate failure. Refer to CHL-I 220

❶ *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 64)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6401											**WRONG PARAMETERS ENTERED** Restart channel wrap routines and enter parameters as listed on MICRO 210 (called for two channel test on single channel only)	
6404 6405		Not Used	Not Used	A-A1Q2 *B-A1C2 *A-B1K2 A-B1T4 *B-A1E6 A-A1S2	*A-B1K2 A-A1S2 A-A1N2 A-B1U4	*A-A1Q2 *B-A1C2 *A-B1K2 A-B1T4 *B-A1E6 A-A1S2 A-B2F2	*A-A1P2 *B-A1C4 *A-B1K2 *B-A1F6 A-A1S2 A-B1T4	*A-A1K2 *B-A1H2 *A-B1K2 *A-A1D2 A-A1S2	*A-A1J2 *B-A1H4 *A-B1K2 *A-A1D4 A-A1S2	0454	**REQUEST IN IS NOT ON WITH "NON-SUPPRESSIBLE REQUEST IN" ON** A CU initiated selection has just been started; Request In should be on to the simulated channel microdiagnostic.	Refer to CHL-I 135
6408 6409		Not Used	Not Used		A-B2L2 *A-A1K2 *A-A1J2	A-B2L2 A-A1R2	A-B2L2 A-A1R2			0434	**CHANNEL A OR B PASS WITH X CHANNEL (CHAN C/D) BRANCH UP**	Refer to CS104 and CHL-I 150 for X channel (channel C/D).
640C 640D		Not Used	Not Used		A-A1R2			*A-A1K2 A-A1R2 *A-A1G2 *A-A1D2 *A-A1H2	*A-A1J2 A-A1R2 *A-A1G4 *A-A1D4 *A-A1H4	043C	**CHANNEL C OR D PASS WITH X CHANNEL (CHAN C/D) BRANCH DOWN**	Refer to CS104 and CHL-I 150 for X channel (channel C/D).
6410 6411		Not Used	Not Used			A-A1R2 A-B2L2 A-B1U4 A-B1M2		A-B2L2 A-B1U4 A-B1M2		0420	**CHANNEL A (C) PASS, CHANNEL B (D) BRANCH IS UP**	Refer to CHL-I 180
6414 6415		Not Used	Not Used				*A-A1P2 *B-A1D4 *B-A1F6 *B-A1C4 A-A1R2 *A-A1Q2 A-B2F2		*A-A1J2 *A-A1G4 *A-A1D4 *A-A1H4 A-A1R2 *A-A1K2 A-B2F2	0424	**CHANNEL B (D) PASS, CHANNEL B (D) BRANCH IS DOWN**	Refer to CHL-I 180
6418 6419		Not Used	Not Used	A-A1Q2 *B-A1E6 *B-A1D2 *A-A1M2 *A-B1L2 A-B2L2 A-A1R2	*A-A1M2 *A-B1L2 A-B2L2 A-A1R2 A-B1U4	*A-A1Q2 *B-A1E6 *B-A1D2 *A-A1M2 A-A1R2 A-B2S2	*A-A1P2 *B-A1F6 *B-A1D4 *A-A1M2 A-A1R2	*A-A1K2 *A-A1D2 *A-A1G2 *A-A1M2 A-A1R2	*A-A1J2 *A-A1D4 *A-A1G4 *A-A1M2 A-A1R2	0464	**SELTD BRANCH FAILED TO COME UP** A CU initiated selection has just been attempted. Request In was received. Select Out and Hold Out were sent from the simulated channel (microdiagnostic).	Refer to CHL-I 220

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Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code ❶	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
641C **641D**		Not Used	Not Used	A-A1Q2 *B-A1C2 A-A1S2 *A-B1L2	A-A1S2 *A-B1L2	*A-A1Q2 *B-A1C2	*A-A1P2 *B-A1C4	*A-A1K2 *A-A1H2	*A-A1J2 *A-A1H4	046C	**OP IN FAILED TO COME UP** During a CU initiated selection, Op In was raised. When checked at the simulated channel (microdiagnostic) it was off.	Refer to KA102 (channel A), KB102 (channel B), KC102 (channel C), KD102 (channel D)
6420 **6421**		Not Used	Not Used	*B-A1F2		*B-A1F2	*B-A1F4	*A-A1E2	*A-A1E4	046C	**MARK IN GATE FAILED TO COME UP** Mark In tag should be active whenever Op In is active. Op In is on at this time.	Refer to AA401 (channel A), BA401 (channel B), CA401 (channel C), DA401 (channel D)
6422 **6423**		Not Used	Not Used	A-A1Q2 *B-A1D2 A-A1S2	A-A1S2 A-B1L2	*A-A1Q2 *B-A1D2	*A-A1P2 *B-A1D4	*A-A1K2 *A-A1G2	*A-A1J2 *A-A1G4	258C	**SELECT IN IS UP** The control unit was selected by a control unit–initiated sequence. Select In was checked and found active.	Refer to CHL-I 220
6424 **6425**		Not Used	Not Used	A-A1Q2 *A-B1K2	*A-B1K2	*A-A1Q2 A-B2S2	*A-A1P2 *A-B1K2 A-B1T4	*A-A1K2 *A-B1K2	*A-A1J2 *A-B1K2	0510 2410	**REQUEST IN NOT ON WITH SUPPRESSIBLE REQUEST IN ON (CHANNEL A, B, C, OR D)** A CU initiated selection has just been attempted. Request In should be on to the simulated channel (microdiagnostic).	Refer to CHL-I 135
6426 **6427**		Not Used	Not Used	A-A1Q2 *B-A1C2 A-A1S2 *A-B1L2	A-A1S2 *A-B1L2	*A-A1Q2 *B-A1C2	*A-A1P2 *B-A1C4	*A-A1K2 *A-A1H2	*A-A1J2 *A-A1H4	2524	**ADDRESS IN DOWN** During a transfer of bus out data, Address In was found to be inactive.	Refer to CHL-I 220
6428 **6429**		Not Used	Not Used	A-A1Q2 *A-A1M2 A-B2L2 A-A1U2	*A-A1M2 A-B2L2 A-A1U2	*A-A1Q2 *B-A1C2 *A-A1M2	*A-A1P2 *B-A1C4 *A-A1M2	*A-A1K2 *A-A1H2 *A-A1M2	*A-A1J2 *A-A1H4 *A-A1M2	2510	**COMMAND OUT IS DOWN** Command Out was raised. When sampled it was found inactive.	Refer to CHL-I 220
642A **642B**		Received Data	Expected Data	*B-A1E2 *B-A1F2 A-A1Q2 *A-A1M2 *A-B2L2	A-A1M2 A-B2L2 A-A1S2 A-A1U2	*B-A1E2 *B-B1F2 *A-A1Q2 *A-A1M2	*B-A1E4 *B-A1F4 *A-A1P2 *A-A1M2	*A-A1F2 *A-A1E2 *A-A1K2 *A-A1M2	*A-A1F4 *A-A1E4 *A-A1J2 *A-A1M2	2560	**BUS OUT PARITY** During a data transfer on bus out, a parity error was detected.	Refer to CHL-I 165

❶ *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 64)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
642C 642D		Received Data	Expected Data	*B-A1E2 *B-A1F2 A-A1T2 A-A1N2	A-A1L2 A-A1M2 A-B1M2 A-A1T2 A-A1N2 A-A1U2 A-A1S2 A-B2N2	A-A1L2 *B-A1E2 *B-A1F2 A-A1N2 A-A1M2	A-A1L2 *B-A1E4 *B-A1F4 A-A1N2 A-A1M2	A-A1L2 *A-A1F2 *A-A1E2 A-A1N2	A-A1L2 *A-A1F4 *A-A1E4 A-A1N2	2560	**WRITE DATA** The received data is not equal to the data sent using Command Out tag to check Write Data Path.	Refer to CHL-I 155 Check A-A1T2 for proper plugging. See INST 25.
6430 6431		Not Used	Not Used	A-A1Q2 *B-A1C2 *A-B1L2	*A-B1L2 A-A1U2	*A-A1Q2 *B-A1C2 A-A1S2	*A-A1P2 *B-A1C4	*A-A1K2 *A-A1H2	*A-A1J2 *A-A1H4	0540	**STATUS IN IS DOWN** During a transfer of bus in data, Status In was found to be inactive.	Refer to CHL-I 220
6438 6439		Received Data	Expected Data	*B-A1E2 *B-A1F2 A-A1T2	A-A1T2 A-B1F2 A-A1U2	*B-A1E2 *B-A1F2	*B-A1E4 *B-A1F4	*A-A1F2 *A-A1E2	*A-A1F4 *A-A1E4	05AC	**BUFFER PARITY CHECK** A buffer parity error was detected in the bus in data path.	Refer to CHL-I 155
643C 643D		Received Data	Expected Data	*B-A1E2 *B-A1F2 A-A1T2	A-B1D2 A-B1U4 A-A1T2	A-A1T2 *A-A1Q2 *B-A1E2 *B-A1F2	*A-A1P2 *B-A1E4 *B-A1F4 A-A1R2 A-A1T2	*A-A1F2 *A-A1E2 A-A1R2	*A-A1F4 *A-A1E4 A-A1R2	05F4	**BUS IN PARITY CHECK** A (CI) bus in parity error was detected in the bus in data path; a buffer parity error was not detected.	Refer to CHL-I 155
6440 6441		Received Data	Expected Data	*B-A1E2 *B-A1F2 A-A1T2	A-A1T2 *A-A1U2 *A-B1F2	*B-A1E2 *B-A1F2 *A-A1Q2 A-A1T2	*B-A1E4 *B-A1F4 A-A1R2 *A-A1P2	*A-A1F2 *A-A1E2	*A-A1F4 *A-A1E4 A-A1R2	05CC	**BUS IN MISCOMPARE CHECK** A bus in miscompare error was detected in the bus in data path.	Refer to CHL-I 155
644C 644D		Received Data	Not Used	A-A1T2	A-A1T2					24E0	**BUFFER PARITY ERROR** The CU presented its hardware jumpered address on bus in, and bad parity was detected.	Refer to CHL-I 155
6450 6451		Received Data	Not Used		A-A1T2 A-A1M2					245C	**BUS IN PARITY ERROR** Bad parity was detected by the simulated channel (micro-diagnostics). No buffer parity error was detected.	Refer to CHL-I 155

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

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Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6458 6459		Not Used	Not Used	A-A1Q2 *B-A1C2		*A-A1Q2 *B-A1C2	*A-A1P2 *B-A1C4	*A-A1K2 *A-A1H2	*A-A1J2 *A-A1H4	2498	**SUPPRESSIBLE REQUEST IN UP** Suppress Out was raised; this should have inhibited Suppressible Request In. When sampled, Suppressible Request In was found active.	Refer to CHL-I 135
6460 6461		Not Used	Not Used	A-B1U4 A-A1Q2	A-B1U4	*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	2594	**SELECT IN IS DOWN** A CU-initiated selection has been attempted and found to be successful. (Select In was down and SELTD branch was active.) Then, a special Op 30 was executed which should have brought up Select In. This is a normal stop for a CU without Intermix or String Switch Attachment feature or hardware EC 437314. Verify features and/or EC, then reload routine 60 and use parameter entry. (See MICRO 210 for parameter bytes.) Program should run error-free.	
6462 6463				A-A1Q2 A-A1T2 *A-A1M2 A-A1L2 A-B1D2	A-A1T2 *A-A1M2 A-A1L2 A-B1D2	*A-A1Q2 *A-A1M2 *A-A1L2	*A-A1P2 *A-A1M2 *A-A1L2	*A-A1K2 *A-A1M2 *A-A1L2	*A-A1J2 *A-A1M2 *A-A1L2		**SECOND ADDRESS SELECTED CHANNEL A OR C** While stepping through addresses a second selection has occurred, on channel A or C, different from the address first selected.	Incorrect parameter entry can cause this error. See Note 1 on MICRO 210.
6464 6465							*A-A1P2 *A-A1M2 *A-A1L2		*A-A1J2 *A-A1M2 *A-A1L2		**SECOND ADDRESS SELECTED CHANNEL B OR D** While stepping through addresses a second selection has occurred, on channel B or D, different from the address first selected.	Incorrect parameter entry can cause this error. See note 1 MICRO 210.
6466 6467					A-A1T2						**NO ADDRESS SELECTED** Called for two channel execution, by parameter, but no address was selected on either channel.	
6468 6469					A-A1T2	*A-A1Q2		*A-A1K2			**ONLY B/D CHANNEL SELECTED** Called through parameters for two channel execution but only channel B/D address was selected.	
646A 646B					A-A1T2		*A-A1P2		*A-A1J2		**ONLY A/C CHANNEL SELECTED** Called through parameters for two channel execution but only channel A/C was selected.	
646C 646D					A-A1T2	*A-A1Q2 *A-A1M2 *A-A1L2 *B-A1C2		*A-A1K2 *A-A1M2 *A-A1L2			**SINGLE CHANNEL ADDRESS NOT ACCEPTED** Called through parameters for single channel operation on channel A/C but no address for that channel was accepted.	
646E 646F					A-A1T2		*A-A1P2 *A-A1M2 *A-A1L2 *B-A1C4		*A-A1J2 *A-A1M2 *A-A1L2		**SINGLE CHANNEL ADDRESS NOT ACCEPTED** Called through parameters for single channel operation on channel B/D but no address for that channel was accepted.	

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 66)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6604 **6605**		Not Used	Not Used	*A-A1M2 A-A1Q2 A-A1U2	A-A1U2 *A-A1M2	*A-A1M2 *A-A1Q2	*A-A1M2 *A-A1P2	*A-A1M2 *A-A1K2	*A-A1M2 *A-A1J2	0424	**HLTIO BRANCH IS ON (CHANNEL A, B, C, OR D)** No attempt has yet been made to bring up Halt I/O. When sampled, it was found on.	Refer to CHL-I 140
6608 **6609**		Received Data	Expected Data '00'	A-A1T2 *A-B1E2 *A-B1M2	A-A1T2 *A-B1E2 *A-B1M2					0428	**NA REG IS NOT PROTECTED** TB Bit 7 was not set on. This should inhibit ingating into the NA register. If NA has anything other than zero when checked, a gating problem exists in the NA register. The gating for the NA register is common to channel A (C) and B (D). Byte 2 and 3 contain the received and expected data, respectively.	Refer to CHL-I 165
660C **660D**		Not Used	Not Used	*B-A1C2 A-A1Q2 A-A1U2	A-A1U2 *A-A1M2 A-B2L2 A-A1T2	*A-A1Q2 *A-A1M2 *B-A1C2 *B-A1E2 *B-A1F2 A-A1T2	*A-A1P2 *A-A1M2 *B-A1C4 *B-A1E4 *B-A1F4 A-A1T2	A-A1K2 *A-A1M2 *A-A1H2 *A-A1F2 *A-A1E4 A-A1T2	*A-A1J2 *A-A1M2 *A-A1H4 *A-A1F4 *A-A1E4 A-A1T2	04A4	**ADDRO BRANCH IS DOWN (CHANNEL A, B, C, OR D)** The ADDRO (Address Out) branch should be up at this time. The CU address was placed on Bus Out; Address Out tag, Hold Out tag, and Select Out tag were all raised. These conditions should result in an ADDRO branch. This error occurs if: 1. The Enable/Disable switch is in the Disable position. 2. The channel microdiagnostics were not run in sequence. (The microdiagnostic depends on previous microdiagnostics to determine the correct address. If these microdiagnostics have not been run, or if they presented the wrong CU address, the address placed on bus out will not compare). 3. Channel A (C) address is the same as channel B (D) address. (Test will not run properly if both addresses are the same. Refer to INST 20 for instructions to change one of them). 4. A bit failure exists on Bus Out. If a receiver is hot or dead, and if it is part of the address scheme, ADDRO will fail to come up because of no address compare. 5. A problem exists with the ADDRO branch or its controls.	Incorrect parameter entry can cause this error. See note 1 on MICRO 210. Refer to CHL-I 165 for Address Compare.
6610 **6611**		Received address on bus out	Expected address on bus out	A-A1T2 *A-B1E2 A-A1L2 A-A1D2 A-A1U2	A-A1T2 *A-B1E2 A-A1L2 A-A1D2 A-A1U2	*A-A1L2	*A-A1L2	*A-A1L2	*A-A1L2	04A4	**ADDRESS ON BUS OUT NOT RECEIVED OK (CHANNEL A, B, C, OR D)** The address was placed in the TA register and then gated to the NA register. If the NA register does not contain the same address, this error is posted.	Refer to CHL-I 165

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**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 66)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6614 6615		Not Used	Not Used	A-A1Q2 *B-A1D2 *B-A1E6		*A-A1Q2 *B-A1D2 *B-A1E6	*A-A1P2 *B-A1D4 *B-A1F6	*A-A1K2 *A-A1G2 *A-A1D2	*A-A1J2 *A-A1G4 *A-A1D4	043C	**SELTD IS DOWN (CHANNEL A, B, C, OR D)** Address Out (with the proper address on bus out, Hold Out, and Select Out have all been received. These conditions should result in a SELTD branch.	Refer to CHL-I 165 for Address Compare
6618 6619		Not Used	Not Used	A-A1Q2 *B-A1D2 A-A1S2	A-A1S2	*A-A1Q2 *B-A1D2	*A-A1P2 *B-A1D4	*A-A1K2 *A-A1G2	*A-A1J2 *A-A1G4	0448	**SELECT IN IS ON (CHANNEL A, B, C, OR D)** Select Out was properly trapped during a selection sequence initiated by a simulated channel. Select In should not be up.	Refer to CHL-I 220
661A 661B		Data Received	Data Expected	A-A1Q2 *B-A1E2 *B-A1F2 A-A1S2	*A-A1M2 A-A1S2	*A-A1Q2 *B-A1E2 *B-A1F2	*A-A1P2 *B-A1E4 *B-A1F4	*A-A1K2 *A-A1F2 *A-A1E2	*A-A1J2 *A-A1F4 *A-A1E4	0448	**BOPAR BRANCH IS ON (CHANNEL A, B, C, OR D)** Bus out parity check branch should be off during initial selection. When sampled it was found active.	Refer to CHL-I 165
661C 661D		Not Used	Not Used	A-A1Q2 *B-A1C2 *A-A1M2		*A-A1Q2 *B-A1C2 *A-A1M2	*A-A1P2 *B-A1C4 *A-A1M2	*A-A1K2 *A-A1H2 *A-A1M2	*A-A1J2 *A-A1H4 *A-A1M2	048C	**ADDRO BRANCH IS ON (CHANNEL A, B, C, OR D)** The ADDRO (Address Out) branch came up properly during initial selection. It failed to drop after Address Out was dropped.	Refer to CHL-I 220
6624 6625		Received Address	Expected Address	A-A1Q2 A-A1T2 *A-A1M2 A-A1L2 A-B1D2	A-A1T2 *A-A1M2 A-A1L2 A-B1D2	*A-A1Q2 *A-A1M2 *A-A1L2 A-A1T2 A-A1R2 *A-A1P2 A-B1R2	*A-A1P2 *A-A1M2 *A-A1L2 A-A1T2	*A-A1K2 *A-A1M2 *A-A1L2 A-A1T2 A-A1R2	*A-A1J2 *A-A1M2 *A-A1L2 A-A1T2	0460	**INCORRECT ADDRESS ON BUS IN (CHANNEL A, B, C, OR D)** During initial selection, the rise of Address In should be accompanied by the correct CU address on bus in. The address was not correct. Display bytes 3 and 4 for received and expected address, respectively. This error occurs if: 1. The address is improperly wired on A-A1Q2 (channel A), A-A1P2 (channel B), A-A1K2 (channel C), A-A1J2 (channel D). 2. A problem exists with the address assembler.	Refer to CHL-I 155 Refer to CHL-I 165

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A; then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 66)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6628 **6629**		Not Used	Not Used		A-A1T2 A-A1S2 A-A1L2	A-A1T2 A-A1L2	A-A1T2 A-A1L2	A-A1L2	A-A1L2	0479	**ADDRESS IN IS DOWN** During initial selection, Address In was raised to load the bus and compare the address. A sample of Address In at this time found it down.	Refer to CHL-I 220
662C **662D**		Not Used	Not Used	A-A1Q2 *A-A1T2	A-A1T2 A-A1L2	*A-A1Q2 A-A1L2	*A-A1P2 A-A1L2	*A-A1K2 A-A1L2	*A-A1J2 A-A1L2	0588	**BUFFER PARITY CHECK** This error indicated bad parity on bus in.	Refer to CHL-I 155
6638 **6639**		Not Used	Not Used	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	0590	**COMMO BRANCH IS DOWN (CHANNEL A, B, C, OR D)** During initial selection, Command Out was just raised. This should result in a COMMO Branch. When sampled, the branch was found off.	See error 6428
663C **663D**		Received data: If 'FF', the gate failed. If not '00' or 'FF., a bit is active in NA register.	Expected Data = '00'		A-B1E2 A-A1T2 A-B1M2					04BC	**BUS OUT NOT ZERO WITH ALLOW NA BIT OFF** 'FF' was placed on bus out, but the NA register was left protected. This should inhibit any data from gating into the NA register. Either the gate failed or a bit is active beyond the gate.	Refer to CHL-I 165 (See also error 6608)
6640 **6641**		If received data = '00'	Expected data = 'FF'	*A-A1L2 A-A1U2 A-A1T2	A-A1U2 A-A1T2 *A-A1L2	*A-A1L2	*A-A1L2	*A-A1L2	*A-A1L2	04B8	**BUS OUT NOT FF WITH ALLOW NA BIT ON (CHANNEL A, B, C, OR D)** 'FF' was placed on bus out, and the NA Allow bit was set. This should have caused 'FF' to ingate into the NA reg. If any bit is off when checked, this error is posted. Display bytes 2 and 3 for received and expected data, respectively.	Refer to CHL-I 165. Bus out did not gate properly.
		If more than one, but not all, data bits are off	Expected data = 'FF'	A-A1U2	A-A1U2					04B8		Refer to CHL-I 165
		If received data has any one of these bits off: 0, 1, 2, 3	Expected data = 'FF'	*A-A1L2 A-A1T2 A-B1E2	A-A1T2 *A-A1L2 A-B1E2	*A-A1L2 A-A1T2	*A-A1L2 A-A1T2	*A-A1L2 A-A1T2	*A-A1L2 A-A1T2	04B8		Refer to CHL-I 165
		If received data has any one of these bits off: 4, 5, 6, 7, it indicates that the P bit failed.	Expected data = 'FF'	*A-A1L2 A-B1E2	A-A1T2 *A-A1L2 A-B1E2	*A-A1L2	*A-A1L2	*A-A1L2	*A-A1L2	04B8		Refer to CHL-I 165

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 66)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6642 6643		Data Received	Data Expected	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	26C0	**BOPAR BRANCH IS ON** Bus Out Parity Check Branch should be off during initial selection. When sampled it was found active.	Refer to CHL-I 165
6644 6645		Not Used	Not Used		A-B1L2 A-A1S2					2658	**ADDRESS IN FAILED TO GO OFF (CHANNEL A, B, C, OR D)** During initial selection, Command Out was raised and Address In was dropped. When sampled, Address In was found on.	Refer to CHL-I 220
6648 6649		Not Used	Not Used	*A-A1M2 A-A1Q2 *B-A1C2		*A-A1M2 *A-A1Q2 *B-A1C2	*A-A1M2 *A-A1P2 *B-A1C4	*A-A1M2 *A-A1K2 *A-A1H2	*A-A1M2 *A-A1J2 *A-A1H4	2614	**COMMO BRANCH IS UP (CHANNEL A, B, C, OR D)** During initial selection, Command Out was raised and then dropped. When sampled, it was still on.	Refer to CHL-I 220
664C 664D		Not Used	Not Used	*A-A1M2 A-A1Q2 A-B2L2 A-A1R2	*A-A1M2 A-B2L2 A-A1R2	*A-A1M2 *A-A1Q2	*A-A1M2 *A-A1P2	*A-A1M2 *A-A1K2	*A-A1M2 *A-A1J2	26A0	**SUPPO BRANCH IS OFF (CHANNEL A, B, C, OR D)** During initial selection, Suppress Out was raised. This should have resulted in a SUPPO branch. When checked, SUPPO branch was found off.	Refer to CHL-I 150
6650 6651		Not Used	Not Used	A-A1Q2 *B-A1C2 *A-B1L2	*A-B1L2	*A-A1Q2 *B-A1C2	*A-A1P2 *B-A1C4	*A-A1K2 *A-A1H2	*A-A1J2 *A-A1H4	2614	**STATUS IN IS NOT UP (CHANNEL A, B, C, OR D)** During initial selection, Status In was raised. When checked at the receiver, it was found off.	Refer to CHL-I 220
6652 6653		Received Status	Expected Status	A-A1Q2 A-A1T2 *A-B1F2	A-A1T2 *A-B1F2	*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	26A4	**STATUS IN OR BUS IN NOT OK (CHANNEL A, B, C, OR D)** During initial selection, a fictitious status ('AA') was placed on Bus In, and Status In was raised. The received status was then checked at the simulated channel but found not equal to 'AA'. Bytes 3 and 4 hold the received and expected status, respectively.	Refer to CHL-I 155 for Bus In and CHL-I 220 for Status In
6654 6655		Received Data	Expected Data		A-A1T2					2674	**BUS IN PARITY ERROR** This error indicates bad parity on CI Bus In.	Refer to CHL-I 155 (See also error 643C)

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 66)

Note: *Error code and message bytes are determined on MICRO 25.*

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code ❶	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6658 **6659**		Not Used	Not Used	A-A1Q2 *A-B1L2	*A-B1L2	*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	267C	**STATUS IN IS ON (CHANNEL A, B, C, OR D)** During initial selection, after the status was sent and Status In was dropped, a check of the in tags revealed that Status In was still up at the receiver.	Refer to CHL-I 220
665C **665D**		Not Used	Not Used	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	264C	**SUPPO BRANCH IS ON (CHANNEL A, B, C, OR D)** During initial selection, Suppress Out was raised and then dropped. At this time, the SUPPO branch should be off.	Refer to CHL-I 150
6660 **6661**		Not Used	Not Used	A-A1Q2 *A-A1M2 *B-A1C2	*A-A1M2	*A-A1Q2 *A-A1M2 *B-A1C2	*A-A1P2 *A-A1M2 *B-A1C4	*A-A1K2 *A-A1M2 *A-A1H2	*A-A1J2 *A-A1M2 *A-A1H4	2650	**SELTD BRANCH IS ON (CHANNEL A, B, C, OR D)** After initial selection, Address Out was raised and Hold Out and Select Out were dropped to force a Halt I/O. This should have caused the SELTD branch to drop.	Refer to CHL-I 220
6664 **6665**		Not Used	Not Used	*A-A1M2 A-A1Q2 A-A1U2 A-B2L2	A-B2L2 *A-A1M2 A-A1U2	*A-A1M2 *A-A1Q2 A-A1R2 A-B1U4	*A-A1M2 *A-A1P2	*A-A1M2 *A-A1K2 A-A1R2	*A-A1M2 *A-A1J2	2660	**HLTIO BRANCH IS OFF (CHANNEL A, B, C, OR D)** After initial selection, Address Out was raised and Hold Out and Select Out were dropped to cause a Halt I/O. This should result in a HLTIO Branch, but none was detected.	Refer to CHL-I 140 for Halt I/O
6668 **6669**		Not Used	Not Used	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	266C	**COMMO BRANCH IS OFF (CHANNEL A, B, C, OR D)** A Halt I/O has just been generated by the simulated channel. This should cause the COMMO branch to come on. When sampled, it was found off.	Refer to CHL-I 220
666C **666D**		Not Used	Not Used	A-A1Q2 *A-A1M2		*A-A1Q2 *A-A1M2	*A-A1P2 *A-A1M2	*A-A1K2 *A-A1M2	*A-A1J2 *A-A1M2	2684	**HLTIO BRANCH IS UP (CHANNEL A, B, C, OR D)** In response to a Halt I/O, the CU caused operational In to drop. This should have caused the HLTIO branch to drop. When sampled, the HLTIO branch was still up.	Refer to CHL-I 140
6670 **6671**		Not Used	Not Used	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	2674	**COMMO BRANCH IS ON (CHANNEL A, B, C, OR D)** At the completion of a Halt I/O, Op In was dropped. This should have resulted in the dropping of the HLTIO branch and the COMMO branch. When sampled, the COMMO branch was still on.	Refer to CHL-I 140 for Halt I/O Refer to CHL-I 220 for COMMO

❶ *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 66)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6674 6675		Not Used	Not Used	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	2678	**ADDRESS IN IS UP (CHANNEL A, B, C, OR D)** Op In and Address In were both up. Op In was then dropped, which should have resulted in Address in going off. It did not.	
6676 6677		Not Used	Not Used	A-A1R2	A-A1R2	A-A1R2	A-A1R2	A-A1R2	A-A1R2	2720	X CHAN/SUPPO branch condition is not operating properly on channel A or B. SUPPO activated the CH14 branch after a SPEC:18. This should gate XCHAN branch which should result in a CH14 zero branch. On Channel C or D SPEC:18 did not activate X CHAN branch.	

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 68)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6804 6805		Address Used	Not Used	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	042C	**SELTD WITH WRONG ADDRESS (CHANNEL A, B, C, OR D)** The SELTD branch came on while the device was intentionally addressed with the wrong address. Display the 3rd byte to find out what address was used. This is a normal stop for a CU with 32 Drive Expansion feature, or 64 drive addressing. Verify that address used is a ligitimate CU address, then reload diagnostic 60 and use parameter entry. (See MICRO 210 for parameter bytes.) Program should run error free.	Refer to CHL-I 220
6808 6809		Address Used	Not Used	A-A1Q2 *B-A1E6 *B-A1D2		*A-A1Q2 *B-A1E6 *B-A1D2	*A-A1P2 *B-A1F6 *B-A1D4	*A-A1K2 *A-A1D2 *A-A1G2	*A-A1J2 *A-A1D4 *A-A1G4	042C	**NO SELECT IN WITH WRONG ADDRESS (CHANNEL A, B, C, OR D)** The simulated channel (microdiagnostic) intentionally addressed the device with the wrong address. This should have caused Select In to propagate back to the channel. When checked, Select In was found off.	Refer to CHL-I 220
680D		Address Used	Not Used		A-A1R2		A-A1R2 *A-A1P2		A-A1R2	0418	**CHANNEL B (D) WITH WRONG ADDRESS** The Channel B branch came on while the device was intentionally addressed with the wrong address. Channel B (D) should not be up when not selected. Display byte 3 to find the address used.	Refer to CHL-I 180
6810 6811		Address Used	Not Used		A-A1R2					04B0	**CHANNEL X (CHANNEL C/D) WITH WRONG ADDRESS** The Channel X branch came on while the device was intentionally addressed with the wrong address. Channel X should not be up when not selected.	Refer to CS104 and CHL-I 150
6820 6821		Not Used	Not Used								Invalid feature parameter entered.	Refer to MICRO 200, 210 for parameter entries.

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 6A)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6A04 **6A05**		Not Used	Not Used	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	052C	**STATUS IN IS NOT ON (CHANNEL A, B, C, OR D)** Status In was raised in the CU to simulate Stacked Status and to force a short busy sequence. When checked, Status In was found off.	Refer to CHL-I 220
6A08 **6A09**		Received Status	Expected Status = '50'	A-A1T2 A-A1Q2	A-A1T2 *A-A1Q2	A-A1T2 *A-A1Q2 *A-A1P2	A-A1T2 *A-A1P2	A-A1T2 *A-A1K2	A-A1T2 *A-A1J2	0500	**STATUS NOT OK (CHANNEL A, B, C, OR D)** During a short busy sequence, status '50' was presented to the simulated channel microdiagnostic. When checked, the status was not as expected. Bytes 2 and 3 hold the received and expected status, respectively.	Refer to CHL-I 155
6A0C **6A0D**		Not Used	Not Used	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	0514	**STATUS IN IS ON AFTER STATUS HAS BEEN PRESENTED (CHANNEL A, B, C, OR D)** Following a short busy sequence, Status In was found to be still active.	Refer to CHL-I 220
6A10 **6A11**		Not Used	Not Used	A-A1Q2 A-A1U2 *A-A1L2 *A-A1M2	A-A1U2 *A-A1L2 *A-B1L2 *A-A1M2	*A-A1Q2 A-A1U2 *A-B1M2 A-A1M2	*A-A1P2 *A-A1M2 *A-B1M2 A-A1T2	*A-A1K2 *A-A1M2 *A-B1M2	*A-A1J2 *A-A1M2 *A-B1M2	05A0	**CUEND NOT UP (CHANNEL A, B, C, OR D)** Following a short busy sequence, the CU was selected and the CUEND branch was checked and found off. It should be on.	Refer to CHL-I 145
6A14 **6A15**		Not Used	Not Used	A-A1Q2		*A-A1Q2 *B-A1E2	*A-A1P2 *B-A1E4	*A-A1K2 *A-A1F2	*A-A1J2 *A-A1F4	0544	**CUEND BRANCH IS UP (CHANNEL A, B, C, OR D)** CUEND status was presented to the simulated channel. This should have caused the CUEND branch to go off. When sampled, it was found on.	Refer to CHL-I 145
6A18		Not Used	Not Used	A-A1R2 *A-B1U4 A-A1Q2 *A-A1K2	A-A1R2 *A-B1U4 *A-A1Q2 *A-A1K2	A-A1R2 *A-B1U4 *A-A1Q2 *A-A1K2	A-A1R2 *A-B1U4 *A-A1Q2 *A-A1K2	A-A1R2 *A-B1U4 *A-A1Q2 *A-A1K2	A-A1R2 *A-B1U4 *A-A1Q2 *A-A1K2	0554	**SELTD WITH CHAN FREEZE (CHANNEL A, B, C, OR D)** 1. This stop will occur if both channels being checked (A and B or C and D) have the same CU address. 2. An attempt has just been made to select a control unit while the other control unit had the Freeze latch on. This should result in no selection. When the SELTD branch was checked, it was found active.	Refer to CS101 and CHL-I 475

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 6A)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6A19		Not Used	Not Used	A-A1R2 *A-B1U4 *A-A1P2 *A-A1J2	A-A1R2 *A-B1U4 *A-A1P2 *A-A1J2	A-A1R2 *A-B1U4 *A-A1P2 *A-A1J2	A-A1R2 *A-B1U4 *A-A1P2 *A-A1J2	A-A1R2 *A-B1U4 *A-A1P2 *A-A1J2	A-A1R2 *A-B1U4 *A-A1P2 *A-A1J2	0554	**SELTD WITH CHAN FREEZE (CHANNEL A, B, C, OR D)** 1. This stop will occur if both channels being checked (A and B or C and D) have the same CU address. 2. An attempt has just been made to select a control unit while the other control unit had the Freeze latch on. This should result in no selection. When the SELTD branch was checked, it was found active.	Refer to CS101 and CHL-I 475
6A1C **6A1D**		Not Used	Not Used	*A-B1U4 A-A1R2	A-A1R2 *A-B1U4					0570	**FAIL TO SELECT FOLLOWING AN UNFREEZE** It was verified that a CU could not be selected with the Freeze latch on in the other CU. When the Freeze latch was dropped, the CU should have selected.	Refer to CS101 and CHL-I 475
6A24 **6A25**		Not Used	Not Used	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	052C	**STATUS IN NOT UP (CHANNEL A, B, C, OR D)** It was verified that the Freeze/Unfreeze switch worked properly in the selection of a CU. This allowed a Stacked Status sequence to be generated. Consequently, Status In should be on. When checked, it was found off.	Refer to CHL-I 220
6A28 **6A29**		Received Status	Expected Status = '50'	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	0500	**STATUS NOT OK (CHANNEL A, B, C, OR D)** During a short busy sequence, status '50' was presented to the simulated channel (microdiagnostic). When checked, the status was not as expected. Bytes 3 and 4 hold the received and expected status, respectively.	Refer to CHL-I 155
6A2C **6A2D**		Not Used	Not Used	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	0514	**STATUS IN IS ON AFTER STATUS HAS BEEN PRESENTED (CHANNEL A, B, C, OR D)** Following a short busy sequence using long term select, Status In was found to be still active.	Refer to CHL-I 220
6A30 **6A31**		Not Used	Not Used	A-A1Q2 A-A1U2	A-A1U2 *A-A1M2	*A-A1Q2 A-A1U2	*A-A1P2 *A-A1M2	*A-A1K2 *A-A1M2	*A-A1J2 *A-A1M2	05A0	**CUEND NOT UP (CHANNEL A, B, C, OR D)** Following a short busy sequence, the CU was selected and the CUEND branch was tested and found off. The branch should be on.	Refer to CHL-I 145

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 6A)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6A34 **6A35**		Not Used	Not Used	A-A1Q2		*A-A1Q2	*A-A1P2	*A-A1K2	*A-A1J2	0544	**CUEND BRANCH IS UP (CHANNEL A, B, C, OR D)** CUEND status has been presented to the simulated channel. This should cause the CUEND branch to go off. When sampled, it was found on.	Refer to CHL-I 145
6A38		Not Used	Not Used	A-A1R2 *A-B1U4 A-A1Q2	A-A1R2 *A-B1U4 *A-A1Q2 *A-A1K2	A-A1R2 *A-B1U4 *A-A1Q2 *A-A1K2	A-A1R2 *A-B1U4 *A-A1Q2 *A-A1K2	A-A1R2 *A-B1U4 *A-A1Q2 *A-A1K2	A-A1R2 *A-B1U4 *A-A1Q2 *A-A1K2	0554	**SELTD WITH CHAN FREEZE (CHANNEL A, B, C, OR D)** 1. This stop will occur if both channels being checked (A and B or C and D) have the same CU address. 2. An attempt has just been made to select a control unit while the other control unit had the Freeze latch on. This should result in no selection. When the SELTD branch was checked, it was found active.	Refer to CHL-I 475
6A39		Not Used	Not Used		A-A1R2 *A-B1U4 *A-A1P2 *A-A1J2	A-A1R2 *A-B1U4 *A-A1P2 *A-A1J2	A-A1R2 *A-B1U4 *A-A1P2 *A-A1J2	A-A1R2 *A-B1U4 *A-A1P2 *A-A1J2	A-A1R2 *A-B1U4 *A-A1P2 *A-A1J2	0554	**SELTD WITH CHAN FREEZE (CHANNEL A, B, C, OR D)** 1. This stop will occur if both channels being checked (A and B or C and D) have the same CU address. 2. An attempt has just been made to select a control unit while the other control unit had the Freeze latch on. This should result in no selection. When the SELTD branch was checked, it was found active.	Refer to CHL-I 475
6A3C **6A3D**		Not Used	Not Used	A-A1R2 *A-B1U4	A-A1R2 *A-B1U4					0570	**FAIL TO SELECT FOLLOWING AN UNFREEZE** It was verified that a CU could not be selected with the Freeze latch on in the other CU. When the Freeze latch was dropped, the CU should have selected.	Refer to CHL-I 475 and CS101
6A40 **6A41**		Not Used	Not Used	*A-A1M2	*A-A1M2					2A40	**COMMO IS UP WITH NO SELECT** With the CU not selected, a command of 'FF' was placed on bus out, and Command Out was raised. The COMMO branch should have been off. When sampled, it was found on.	Refer to CHL-I 220
6A44 **6A45**		Received Data	Expected Data = '00'	A-A1T2	A-A1T2					2A54	**COMMAND OUT DEGATING FAILED (CHANNEL A, B, C, OR D)** 'FF' was placed on bus out, and Command Out was raised. The NA register was then inspected to verify that nothing gated into it. It was not equal to '00'. Display bytes 2 and 3 for received and expected data, respectively.	Refer to CHL-I 220

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

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Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync** Address (Hex)	Error Description	Additional Action and Reference Notes
Error Code ❶	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6C04 **6C05**		Not Used	Not Used	A-A1U2 *A-B1L2	A-A1U2 *A-B1L2					2B04	**XFER BRANCH IS UP (CHANNEL A, B, C, OR D)** XFER branch was sampled and found on when it should have been off.	Refer to CHL-I 140
6C08 **6C09**		Not Used	Not Used	A-A1U2 *A-B1L2 A-A1U2 A-B2K2 A-B2H2	A-A1U2 *A-B1L2 A-A1U2 A-B2K2 A-B2H2					2B04	**XFER BRANCH IS OFF (CHANNEL A, B, C, OR D)** XFER branch was sampled and found off when it should have been on.	Refer to CHL-I 140
6C0C **6C0D**		Not Used	Not Used	A-A1U2 *A-B1L2	A-A1U2 *A-B1L2					2B10	**BFRDY BRANCH IS ON (CHANNEL A, B, C, OR D)** BFRDY (Buffer Ready) branch was found on when it should have been off.	Refer to CHL-I 145
6C10 **6C11**		Not Used	Not Used	A-A1U2 *A-B1L2 *B-A1C2 *A-A1M2	A-A1U2 *A-B1L2 *A-A1M2 A-A1S2	*B-A1C2 *A-A1M2	*B-A1C4 *A-A1M2	*A-A1H2 *A-A1M2	*A-A1H4 *A-A1M2	2B1C	**BFRDY BRANCH IS OFF** BFRDY (Buffer Ready) branch was found off when it should have been on.	Refer to CHL-I 145
6C14 **6C15**		Not Used	Not Used	*B-A1C2 A-A1U2 *A-B1L2	A-A1U2 *A-B1L2	*B-A1C2	*B-A1C4	*A-A1H2	*A-A1H4	2BF4	**DATA IN TAG IS ON (CHANNEL A, B, C, OR D)** Data In tag was found on when it should have been off.	Refer to CHL-I 35
6C18 **6C19**		Not Used	Not Used	*B-A1C2 A-A1U2 *A-B1L2	A-A1U2 *A-B1L2	*B-A1C2	*B-A1C4 A-A1S2	*A-A1H2	*A-A1H4	2BF4	**DATA IN TAG IS OFF (CHANNEL A, B, C, OR D)** Data In tag was found off when it should have been on.	Check jumper on A-A1U2. See INST 16. Refer to CHL-I 35
6C1C **6C1D**		Not Used	Not Used	*B-A1C2 A-A1U2 *A-B1L2	A-A1U2 *A-B1L2	*B-A1C2	*B-A1C4	*A-A1H2	*A-A1H4	2B40	**SERVICE IN TAG IS ON (CHANNEL A, B, C, OR D)** Service In tag was found on when it should have been off.	Refer to CHL-I 35
6C20 **6C21**		Not Used	Not Used	*B-A1C2 A-A1U2 *A-B1L2	A-A1U2 *A-B1L2	*B-A1C2	*B-A1C4	*A-A1H2	*A-A1H4	2B40	**SERVICE IN TAG IS OFF (CHANNEL A, B, C, OR D)** Service In tag was found off when it should have been on.	Refer to CHL-I 35

❶ *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

***Sync on 2CXX (XX = 5th byte) and delayed sync on address '2B04', etc., to verify condition described in Error Description column.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 6C)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync** Address (hex)	Error Description	Additional Action and Reference Notes
Error Code ❶	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6C24 **6C25**		Not Used	Not Used	*A-A1M2 *B-A1E2 *B-A1C2 A-A1S2	A-A1S2 *A-A1M2	*A-A1M2 *B-A1E2 *B-A1C2	*A-A1M2 *B-A1E4 *B-A1C4	*A-A1M2 *A-A1F2 *A-A1H2	*A-A1M2 *A-A1F4 *A-A1H4	2B54	**SERVO BRANCH IS ON WHEN IT SHOULD BE OFF** SERVO (Service Out) branch was sampled and found on when it should have been off.	Refer to CHL-I 180
6C28 **6C29**		Not Used	Not Used	A-A1S2 *A-A1M2 *B-A1E2 *B-A1C2	A-A1S2 *A-A1M2	*A-A1M2 *B-A1E2 *B-A1C2	*A-A1M2 *B-A1C4 *B-A1E4	*A-A1M2 *A-A1F2 *A-A1H2	*A-A1M2 *A-A1F4 *A-A1H4	2B58	**SERVO BRANCH IS OFF WHEN IT SHOULD BE ON** SERVO (Service Out) branch was found off when it should have been on.	Refer to CHL-I 180
6C2C **6C2D**		Not Used	Not Used	A-A1Q2 *B-A1E2 *B-A1F2 *A-A1M2 A-A1S2	*A-A1M2 A-A1S2 A-A1U2	*A-A1Q2 *B-A1E2 *B-A1F2 *A-A1M2	*A-A1P2 *B-A1E4 *B-A1F4 *A-A1M2	*A-A1K2 *A-A1F2 *A-A1E2 *A-A1M2	*A-A1J2 *A-A1F4 *A-A1E4 *A-A1M2	2B4C	**BOPAR BRANCH IS ON** The BOPAR (Bus Out Parity Check) branch came on while good data was being placed on bus out.	Refer to CHL-I 165
6C30 **6C31**		Received Data	Expected Data	A-A1U2 *B-A1E2 *B-A1F2	A-A1U2	*B-A1E2 *B-A1F2	*B-A1E4 *B-A1F4	*A-A1F2 *A-A1E2	*A-A1F4 *A-A1E4	2B74	**BUS IN GATING FAILED** The received data was compared with the expected data and a mismatch was found. Display bytes 3 and 4 for received and expected data, respectively.	Refer to CHL-I 155
6C32 **6C33**		Not Used	Not Used	A-A1T2 A-A1S2	A-A1T2 A-A1S2	A-A1T2	A-A1T2	A-A1T2	A-A1T2	2D68	**NO CHECK 2** Interface control check was forced. This should have caused a Check 2 but did not.	Refer to PANEL 50
6C34 **6C35**		Received Data	Expected Data	*A-A1L2 A-A1T2 A-B1E2 A-A1U2	*A-A1L2 A-A1T2 A-B1E2 A-A1U2	*A-A1L2	*A-A1L2	*A-A1L2	*A-A1L2	2B88 2EE0	**BUS OUT NOT RECEIVED OK (CHANNEL A, B, C, OR D)** The bus out data received was not as expected. Display bytes 3 and 4 for received and expected data, respectively. If program passes through '2EE8' address.	Refer to CHL-I 165
6C36 **6C37**		Not Used	Not Used	A-A1Q2 A-A1T2 A-A1U2	A-A1T2 A-A1U2	*A-A1Q2 A-A1T2 A-A1N2	*A-A1P2 A-A1T2 A-A1N2	*A-A1K2 A-A1T2	*A-A1J2 A-A1T2	2D88	**NO INTERFACE CONTROL CHECK** More than one channel tag was raised. These should have caused an interface control check, but did not.	Refer to CHL-I 185

❶ *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

***Sync on 2CXX (XX = 5th byte) and delayed sync on address '2B54', etc., to verify condition described in Error Description column.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 6C)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync** Address	Error Description	Additional Action and Reference Notes
Error Code ❶	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6C38 **6C39**		Received Data	Expected Data	A-A1T2 *B-A1E2 *B-A1F2 A-A1U2	A-A1T2 A-A1U2	*B-A1E2 *B-A1F2 A-A1T2	*B-A1E4 *B-A1F4	*A-A1F2 *A-A1E2	*A-A1F4 *A-A1E4	2B94	**BUFFER PARITY CHECK** During a Read operation, a Buffer Parity check was detected as different data patterns were put through the buffer and bus in drivers. Display bytes 3 and 4 for received and expected data, respectively.	Refer to CHL-I 155
6C3C **6C3D**		Not Used	Not Used	A-A1T2 A-B2H2 A-A1U2	A-A1T2 A-B2H2 A-A1U2	A-A1L2	A-A1L2	A-A1L2	A-A1L2	2BE8	**BUFFER PARITY CHECK** During a Write operation, bad parity was detected on bus out. This caused the buffer error.	Refer to CHL-I 155
6C3E **6C3F**		Not Used	Not Used	A-A1S2 A-A1U2 A-A1T2 A-B1E2	A-A1S2 A-A1U2 A-A1T2 A-A1E2					2BC0	**XFER CHECK IS ON** An XFER (Transfer) Check was detected while doing a Read or Write operation.	Refer to CHL-I 180
6C40 **6C41**		Not Used	Not Used	A-A1S2 A-A1U2	A-A1S2 A-A1U2					2BB4	**XFER CHECK IS DOWN** An XFER (Transfer) Check was forced during a Read or Write operation. When sampled, it was found inactive.	Refer to CHL-I 180
6C42 **6C43**		Not Used	Not Used	A-A1E2 A-A1S2 A-A1U2 A-A1T2	A-A1S2 A-A1U2 A-A1T2 A-A1E2					2F64	**XFER CHECK IS ON (CHECK A, B, C, OR D)** During a Read Truncation or Write Overrun operation or Halt I/O, a XFER (Transfer) Check was detected.	Refer to CHL-I 180
6C44 **6C45**		Not Used	Not Used	A-A1S2 A-A1T2 A-A1U2 A-B1E2	A-A1T2 A-A1S2 A-A1U2 A-B1E2					2F64	**XFER CHECK FAILED TO COME UP (CHANNEL A, B, C, OR D)** A XFER Check was forced by placing bytes of data into the buffers and not transferring them out. When sampled, the XFER Check was off.	Refer to CHL-I 180
6C48 **6C49**		Not Used	Not Used	A-A1T2 A-A1S2 A-A1U2 A-A1E2	A-A1S2 A-A1U2 A-A1T2 A-A1E2					2F64	**XFER CHECK IS ON (CHANNEL A, B, C, OR D)** A XFER (Transfer) Check was detected while doing a Read Truncation or Halt I/O operation.	Refer to CHL-I 180

❶ *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 -- 909 for common part numbers.*

***Sync on 2CXX (XX = 5th byte) and delayed sync on address '2B94', etc., to verify condition described in Error Description column.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 6C)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync ** Address	Error Description	Additional Action and Reference Notes
Error Code ❶	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6C4C 6C4D		Received Data	Expected Data	A-A1T2	A-A1T2					2FE4	**BUS OUT NOT OK (CHANNEL A, B, C, OR D)** Address Out was raised by the simulated channel (micro-diagnostic) to force a Halt I/O sequence. The NA register was then checked to ensure that no data was gated from bus out. Display bytes 3 and 4 for received and expected data, respectively.	Refer to CHL-I 165
6C50 6C51		Received Data	Expected Data	*B-A1E2 *B-A1F2 A-A1U2	A-A1U2	*B-A1E2 *B-A1F2	*B-A1E4 *B-A1F4	*A-A1F2 *A-A1E2	*A-A1F4 *A-A1E4	2FA4	**BUS IN NOT DEGATED** MD register was gated to bus in when it should not have been.	Refer to CHL-I 155
6C54 6C55		Received Data	Expected Data	A-A1U2 *B-A1E2 *B-A1F2	A-A1U2	*B-A1E2 *B-A1F2	*B-A1E4 *B-A1F4	*A-A1F2 *A-A1E2	*A-A1F4 *A-A1E4	2FA8	**BUS IN NOT OK OR DATA IN/SERVICE IN IS UP (CHANNEL A, B, C, OR D)** Operational In gate was dropped, which should have resulted in inhibiting these in tags and bus in. If bus in does not equal '00', or Data In and Service In are not off, this error occurs.	Refer to CHL-I 155
6C56				A-A1U2	A-A1U2						**SELECTION COMPLETE – DATA NOT UP** Selection has been completed, channel write mode is set and offset interlock is on but Data In is not up. Also return to this check via CA decode at the NA register if test below (6C58) is successful.	
6C58				A-A1U2	A-A1U2						**SERVICE IN IS NOT UP** Sequence shown in 6C56 has been successfully completed (Data In was up) then a switch to service in (CA decode of NA register) has been executed but service in is not up.	Check jumper on A-A1U2. Refer to INST 16.
6C5A				A-A1S2 A-A1U2	A-A1S2 A-A1U2						**BUFFER READY UP** Successful completion of Data In/Service In test sequence is followed by a switch to Channel Read mode. Data Out then Service Out is raised and Buffer Ready has been detected to be up.	Check jumpers on A-A1S2. Refer to INST 16.

❶ *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

***Sync on 2CXX (XX = 5th byte) and delayed sync on address '2FE4', etc., to verify condition described in Error Description column.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 6E)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6E04 **6E05**		Not Used	Not Used	A-A1Q2 *A-A1M2 *B-A1C2 A-B2P2 A-B2T2	A-B2P2 *A-A1M2 A-B2T2 A-A1S2 A-A1R2	*A-A1Q2 *A-A1M2 *B-A1C2	*A-A1P2 *A-A1M2 *B-A1C4	*A-A1K2 *A-A1M2 *A-A1H2	*A-A1J2 *A-A1M2 *A-A1H4	0420	**NO SELECTIVE RESET (CHANNEL A, B, C, OR D)** This error will occur if the Operation Mode switch is not in the Forced Logging position, or a Selective Reset was caused by dropping Operational Out while keeping Suppress Out up. If the Selective Reset worked properly, a branch to location '40' would have occurred. No such branch took place.	Refer to CHL-I 190
6E08 **6E09**		Not Used	Not Used	*A-A1M2 A-A1S2	*A-A1M2 A-A1S2					04C4	**OPERATIONAL IN FAILED TO DROP (CHANNEL A, B, C, OR D)** Following a Selective Reset, it was discovered that Operational In failed to drop.	Refer to CHL-I 220
6E0C **6E0D**		Not Used	Not Used	A-A1S2 *B-A1D2	A-A1S2	*B-A1D2	*B-A1D4	*A-A1G2	*A-A1G4	04AC	**DISCONNECT IN IS UP (CHANNEL A, B, C, OR D)** Following a Selective Reset, Disconnect In should be off. When sampled, it was found active.	Refer to CHL-I 130
6E10 **6E11**		Not Used	Not Used	*B-A1D2 A-A1S2	A-A1S2	*B-A1D2 A-A1S2	*B-A1D4 A-A1S2	*A-A1G2 A-A1S2	*A-A1G4 A-A1S2	0454	**DISCONNECT IN FAILED TO COME UP (CHANNEL A, B, C, OR D)** The microdiagnostic forced a Check 1 error. This should have caused the CU to raise Disconnect In. When checked, the Disconnect In tag was off.	Refer to CHL-I 130
6E24 **6E25**		Not Used	Not Used	A-A1Q2 *B-A1C2 *A-A1M2 A-B2P2	*A-A1M2 A-B2P2	*A-A1Q2 *B-A1C2 *A-A1M2	*A-A1P2 *B-A1C4 *A-A1M2	*A-A1K2 *A-A1H2 *A-A1M2	*A-A1J2 *A-A1H4 *A-A1M2	0420	**NO SELECTIVE RESET (CHANNEL A, B, C, OR D)** A Selective Reset was caused as a result of a Disconnect In sequence. With the CU selected, a Check 1 was forced up. This caused the Disconnect In sequence, which should have caused a Selective Reset to occur. None occurred.	Refer to CHL-I 190
6E28 **6E29**		Not Used	Not Used	*A-A1M2 A-A1S2	*A-A1M2 A-A1S2					04C4	**OPERATIONAL IN FAILED TO DROP (CHANNEL A, B, C, OR D)** Following a Selective Reset, which resulted from a Disconnect In sequence while selected, the CU failed to drop Operational In.	Refer to CHL-I 220

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

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CHANNEL WRAPAROUND ERROR CODE DICTIONARY (ROUTINE 6E)

Note: Error code and message bytes are determined on MICRO 25.

CE Panel Lamp Display				Possible Failing Replaceable Units						Sync Address (hex)	Error Description	Additional Action and Reference Notes
Error Code (1)	Test No. 2ND BYTE	3RD BYTE	4TH BYTE	Single Chan Machine	More Than 1 Chan Fails	Only Channel A Fails	Only Channel B Fails	Only Channel C Fails	Only Channel D Fails			
6E2C 6E2D		Not Used	Not Used	A-A1S2	A-A1S2					04AC	**DISCONNECT IN IS UP (CHANNEL A, B, C, OR D)** Following a Selective Reset, which resulted from a Disconnect In sequence while selected, the CU failed to drop Disconnect In.	Refer to CHL-I 130
6E30 6E31		Not Used	Not Used	A-A1S2 A-B1U4	A-A1S2 A-B1U4					0454	**DISCONNECT IN FAILED TO COME UP** The microdiagnostic forced a Check 1 error. This should have caused the CU to raise Disconnect In. When sampled, it was found inactive.	Refer to CHL-I 130
8100											This is the normal display while looping a selected test.	

(1) *All even numbered error codes are channel A or C failures, and each following odd number refers to the related channel B or D failure. To isolate the problem to one channel, set up options to run each channel alone, starting with channel A, then B, C, and D. If unrelated errors occur while running channels B, C, or D, ignore them and return to the first failure.*

**This is a multiple usage card. Refer to START 900 – 909 for common part numbers.*

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CONTROL UNIT FUNCTION TESTS (Part 1 of 2)

Routine No.	Microdiagnostic Routines	Options (See MICRO 16)	Parameter Entries: BYTE NO.	Parameter Entries: DEFAULT VALUE	Parameter Entries: RANGE AVAILABLE	Comments
82	**REGISTER TEST** This test first checks the SA, SB, SC, and SD registers by resetting them to '00' and then incrementing them until a carry occurs. When the carry occurs, they should be '00' again. Test patterns of '00', 'FF', '01', 'AA', and '55' are then inserted into the SA register and transferred to each of the other registers and compared. This operation is repeated 256 times.	**Loop Options** '02' Bypass Loop Count '04' Inhibit Link '32' Loop Program **Error Control Options** '01' Continue on Error '3A' Loop on First Error '3E' Halt on Error				Routine 82 does not provide standard error message displays. If the program does not complete within 15 seconds the program may be looping. See MICRO 405 for diagnostic procedure. **Operating Instructions:** 1. Operation Mode switch to Forced Logging. 2. Enter/Display switch to Program Data Entry/Display. 3. Data Enter switches to '82' and operate Execute switch. 4. If other than default options are desired, enter them when stop at 'C082' occurs. See MICRO 15, 16 for details of entering options. For default options skip this step. 5. To start program set Data Entry switches to '38' and operate Execute switch. Normal stop without options is 'C484'. Check 2 light is on during execution of this program.
84	**CONTROL UNIT CHECKERS TEST** This test forces certain Check 1 and Check 2 errors to test the ability of the checking circuits to detect them. Not all Check 1 and Check 2 errors can be forced. The program uses diagnostic selective resets and restarts to permit automatic operation – each forced Check 1 is reset and the clock restarted under diagnostic program control.					This test must be run in Forced Logging mode, otherwise a clock stop and Check 1 error will occur. Forced Logging allows diagnostic program control to permit automatic operation. To recover from this stop, operate Check Reset and Start switches. When '8407' error code appears, change Mode switch to Forced Logging and restart routine. If Clock Stop and Check 1 error occurs while in forced logging mode use error code '84xx'. See MICRO 410-420 for error codes. **Operating Instructions:** 1. Operation Mode switch to Forced Logging. 2. Enter/Display switch to Program Data Entry/Display. 3. Data Entry switches to '84' and operate Execute switch. 4. If other than default options are desired, enter them when stop at 'C084' occurs. See MICRO 15, 16 for details on entering options. For default options skip this step. 5. To start program set Data Entry switches to '38' and operate Execute Switch. Normal stop without options is 'C484'.
86	**ALU AND BRANCH TEST** All ALU operations are tested, using data such that all circuits used in the functions are exercised. All branching conditions are set, reset, and tested for proper operation of the branching function. Interface(s) must be disabled when running this diagnostic. a. 'FF' is ANDed with '00'. The expected result is '00'. If not, BAR = '0410'. b. '55' is exclusive ORed with '55'. The expected result is '00'. If not, BAR = '0418'. c. One bit is shifted left in a register by adding the register to itself, until a carry out occurs. Carry and D Bus Equal Zero are expected to occur together. If not, BAR = '0424' or '0428'. d. '01' is added to 'FF' with Store Carry on. Carry and ST3C on are expected to occur together. If not, BAR = '0430', '0434', or '0438'. e. With 'ST3C' on 'FF' is added to '00' with Carry In active. The expected result is '00', if not, BAR = '0440'. f. '01' is added to a previously cleared register until a carry out occurs. g. '01' is added to another register each time a carry out from test F occurs; then test F is repeated until a carry out occurs from the second register. Before each add in test F, the two registers are added together (but without altering them), so that when test G ends with a carry out from the second register, all possible sums and carries in the adder have been exercised. *(Continued on MICRO 402)*					Routine 86 does not provide standard error message displays. If an error loop, clock stop or a Check 1 error occurs, refer to Error Dictionary on MICRO 425. **Operating Instructions:** *Note: Disable interfaces to run this test.* 1. Operation Mode switch to Forced Logging. 2. Enter/Display switch to Program Data Entry/Display. 3. Data Entry switches to '86' and operate Execute switch. 4. If other than default options are desired, enter them when stop at 'C086' occurs. See MICRO 15, 16 for details on entering options. For default options skip this step. 5. To start program set Data Entry switches to '38' and operate Execute switch. Normal stop without options is 'C484'.

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Routine No.	Microdiagnostic Routine	Control Options (from MICRO 16)	Parameter Entries			Comments
			Byte No.	Default Value	Range Available	
86 *(continued from MICRO 400)*	h. Tests the OR function with the following inputs: 1. 'FF' OR 'FF' = 'FF' 2. '00' OR 'FF' = 'FF' 3. 'FF' OR '00' = 'FF' If any test does not result in 'FF', BAR = '0470' or '0478'. j. Tests that '00' OR '00' = '00'. If not, BAR = '0480'. k. Tests that '7E' + '01' + Carry In = '80'. If not, BAR = '0488'. l. Tests that ' FE' - 'FD' + No Carry In = '00'. If not, BAR = '0490' + '02' + (no Carry In) = '00'. m. Tests that a DNST21 statement in the test L operation leaves ST2 off. If not, BAR = '04F8'. n. By dynamically altering a functional word, all BR branch bits and all ST bits except ST1 and ST4 are set, reset, and tested for proper branching. If a failure occurs, BAR = '05D4' or '05D8'. The content of SD register will determine which branch failed. Error Dictionary entry = '8A' (BAR) (SD register). p. The CS field of a functional word is dynamically altered so that each ST bit (except ST4) is set by a 1 to ST bit statement. The ST register is then tested for '11110111'. If not, BAR = '0568'. q. The CS field of a functional word is dynamically altered so that each ST bit (except ST4) is reset by a 0 to ST bit statement. The ST register is then tested for '0000x000'. If not, BAR = '0578'.					
8A	**CE PANEL TEST** This test checks all CE panel options and functions.					See MICRO 427 and 428 for run procedures. If difficulty is encountered running this test, go to PANEL 30 for manual checkout.

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Routine No.	Microdiagnostic Routine	Options (See MICRO 16)	Parameter Entries			Comments
			Byte No.	Default Value	Range Available	
88	**STORAGE SCAN** This test reads a storage location, saves the information in '05E0', and then tests the storage location by writing '00', 'FF', 'AA', and incrementing 1-bits through each bit position. The location is read out and compared following each write. The saved information in '05E0' is then restored to its original location. This procedure is followed until each storage location of the lower 4K is tested. Locations above 4K are tested without saving the original data in the location. The program tailors itself to the correct control storage size.	*Note 1:* *Set to highest available address. See INTR 005 or MFI (hardcard) to determine storage size.*	1 2 3 4 5	'20' '00' '00' Note 1 'FC'	'01'-'FF' '00'-7F' '00'-'FC' '00'-7F' '00'-'FC'	Number of times to loop test. High order of beginning address. Low order of beginning address. High order of ending address. Low order of ending address. **Operating Instructions:** 1. Operation Mode Switch to Forced Logging. 2. Enter Display Switch to Program Data Entry. 3. Data Entry Switches to '88' and operate Execute Switch. 4. If other than default options are desired, enter them when stop at 'C088' occurs. For default options, skip this step. 5. To start program set Data Entry Switches to '38' and operate Execute Switch. Normal stop without options is 'C484'. Refer to MICRO 430 for Error Code Dictionary.
96	**'F' REGISTERS – CONTROL TEST** This test checks the operation of the 'F' registers (TF, GF, NF, and MF). Each of the 32 addressable register of GF, NF, and MF are checked for addressability and bit pattern acceptability. The TF register is checked for addressability control of GF, NF, and MF. The stepping of the TF address register (Bits 3-7) is checked when executing instruction using MF and TA registers.					**Operating Instructions:** 1. Operation Mode Switch to Forced Logging. 2. Enter/Display Switch to Program Data Entry/Display. 3. Data Entry Switches to '96' and operate execute switch. 4. If other than default options are desired, enter them when stop at C096' occurs. See MICRO 15, 16 for details on entering options. For default options, skip this step. 5. To start program, set Data Entry Switches to '38' and operate execute switch. 6. If Check 1 error occurs use FSI 30. Normal stop without options is 'C484'.

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (CONTROL UNIT ROUTINE 82)

ROUTINE 82 - REGISTER TEST	BAR (Hex)	Check-1 Register bit 0	1	2	3	A Reg 4	B Reg 5	6	7	Error Description Failing Register	Possible Failing Replaceable Units
Register Tests Read additional information under "Additional Action and Reference Notes." The sequence is as shown in BAR.	041C	0	X	X	X	X	X	X	X	Zero was added to zero and the results were placed on the D Bus (0 + 0 → D). The D Bus should have gone to '00', but when checked, it was not at '00'. The problem may be a 'hot' bit on A Bus, B Bus, or D Bus.	A-B1J2 A-B1H2 A-B1N2
	0424 0428	0	X	X	X	0	1	X	X	SA register ❶	*A-B2D2
	042C									SA register ❷	*A-B2D2
	0434 0438	0	X	X	X	0	1	X	X	SB register ❶	*A-B2E2
	043C									SB register ❷	*A-B2E2
	0444 0448	0	X	X	X	0	1	X	X	SC register ❶	*A-B2D2
	044C									SC register ❷	*A-B2D2
	0454 0458	0	X	X	X	0	1	X	X	SD register ❶	*A-B2E2
	045C									SD register ❷	*A-B2E2
	0504	0	X	X	X	1	0	X	X	GA register. See ❸ on MICRO 406	*A-B1E2
		0	X	X	X	0	1	X	X	SA register. See ❺ on MICRO 406	*A-B2D2 A-B2G2 A-B2J2 A-B2H2 A-B2L2 *A-B1G2

Additional Action and Reference Notes

PROGRAM DETECTED ERRORS

These routines cause the control unit to stop. When a stop occurs, perform the following:

1. Set Enter/Display switch to Program Data Entry/Display. Bits 8 through 15 specify the failing routine.
2. Set Enter/Display switch to BAR. Bits 0 thru 15 are the instruction address of the stop-or-failing instruction.
3. Use the routine and the instruction address (BAR) to locate a failing unit from the listing.

HARDWARE DETECTED ERRORS

Hardware detected errors cause the control unit to stop with the Check 1 light turned on.

1,2. Steps 1 and 2 are the same as the above steps 1 and 2 for program detected errors.
3. Set Enter/Display switch to Check 1 Reg. Bits 0-15 are the Check 1 register.
4. Use the routine, the failing instruction address (BAR), and the contents of the Check 1 register to locate the FRU.

PROGRAM LOOP

Determine if the program is in a loop by operating the Stop/SI switch. Each subsequent operation of this switch will execute one microprogram step. If in a loop, perform the steps listed under Program Detected Errors.

❶ The failing register is reset to '00' and then incremented by +1 until a carry occurs. This error indicates that a carry failed to occur. The problem may be that the failing register is not gating onto the B bus or that the D bus is not gating into the failing register.

a. Swap cards for symptom change
b. Scope failing register input and output.

❷ The failing register is incremented by +1 until a carry occurs. At that time, the register should be equal to '00', but is not.

a. Swap cards for symptom change
b. Scope the failing register by looping in check bypass.

*Multiple Usage Card

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ROUTINE 82 - REGISTER TEST	BAR (Hex)	Check-1 Register bit 0	1	2	3	A Reg 4	B Reg 5	6	7	Error Description Failing Register	Possible Failing Replaceable Units
Register Tests Read additional information under "Additional Action and Reference Notes" on MICRO 405.	0508									GA register (4)	*A-B1E2
	050C	0	X	X	X	1	0	X	X	TB register (3)	*A-B1M2
		0	X	X	X	0	1	X	X	GA register (5)	*A-B1E2
	0510									TB register (4)	*A-B1M2
	0514	0	X	X	X	1	0	X	X	NC register (3)	*A-B1L2
		0	X	X	X	0	1	X	X	TB register (5)	*A-B1M2
	0518									NC register (4)	*A-B1L2
	051C	0	X	X	X	1	0	X	X	TD register (3)	*A-B1F2
		0	X	X	X	0	1	X	X	NC register (5)	*A-B1L2
	0520									TD register (4)	*A-B1F2
	0524	1	X	X	X	X	X	X	X	TB register (3)	A-B1D2
		0	X	X	X	1	0	X	X	MA register (3)	*A-B1E2 A-A1M2
		0	X	X	X	0	1	X	X	TD register (5)	*A-B1F2
	0528									MA register (4)	*A-B1E2
	052C	0	X	X	X	1	0	X	X	NB register (3)	*A-B1M2 A-B3D2
		0	X	X	X	0	1	X	X	MA register (5)	*A-B1E2 A-A1M2
	0530									NB register (4)	*A-B1M2
	0534	0	X	X	X	1	0	X	X	TC register (3)	*A-B1L2
		0	X	X	X	0	1	X	X	NB register (5)	*A-B1M2 A-B3D2
	0538									TC register (4)	*A-B1L2
	053C	0	X	X	X	1	0	X	X	GB register (3)	*A-B1M2
		0	X	X	X	0	1	X	X	TC register (5)	*A-B1L2
	0540									GB register (4)	*A-B1M2

(3) The microdiagnostic was able to successfully set a pattern into the failing register, but an error occurred when it tried to gate that register onto the A Bus.

The pattern is in the SA register.

(4) The microdiagnostic transferred the contents of a good register into the failing register, but an error was not detected until it compared these two registers. This type of error would indicate that multiple bits are failing, for if only one bit failed a Check 1 should have occurred.

The pattern used is in the SA register.

(5) The microdiagnostic was able to successfully set a pattern into the failing register. It was also able to gate that register onto the A Bus, but an error occurred when it tried to gate that register onto the B Bus.

The pattern used is in the SA register.

*Mutliple Usage Card

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (CONTROL UNIT ROUTINE 82)

ROUTINE 82 - REGISTER TEST	BAR (Hex)	Check-1 Register bit 0	1	2	3	A Reg 4	B Reg 5	6	7	Error Description Failing Register	Possible Failing Replaceable Units
Register Tests Read additional information under "Additional Action and Reference Notes" on MICRO 405.	0544	0	X	X	X	1	0	X	X	MC register ③	*A-B1L2
		0	X	X	X	0	1	X	X	GB register ⑤	*A-B1M2
	0548									MC register ④	*A-B1L2
	054C	0	X	X	X	1	0	X	X	ND register ③	*A-B1F2, A-B1D2
		0	X	X	X	0	1	X	X	MC register ⑤	*A-B1L2
	0550									ND register ④	*A-B1F2
	0554	0	X	X	X	1	0	X	X	MB register ③	*A-B1M2
		0	X	X	X	0	1	X	X	ND register ⑤	*A-B1F2, A-B1D2
	0558									MB register ④	*A-B1M2
	055C	0	X	X	X	1	0	X	X	NA register ③	*A-B1E2, A-A1T2
		0	X	X	X	0	1	X	X	MB register ⑤	*A-B1M2
	0560									NA register ④	*A-B1E2
	0564	0	X	X	X	1	0	X	X	MD register ③	*A-B1F2
		0	X	X	X	0	1	X	X	NA register ⑤	*A-B1E2, A-A1T2
	0568									MD register ④	*A-B1F2
	056C	0	X	X	X	1	0	X	X	GC register ③	*A-B1L2
		0	X	X	X	0	1	X	X	MD register ⑤	*A-B1F2
	0570									GC register ④	*A-B1L2
	0574	0	X	X	X	1	0	X	X	TA register ③	*A-B1E2
		0	X	X	X	0	1	X	X	GC register ⑤	*A-B1L2

③ The microdiagnostic was able to successfully set a pattern into the failing register, but an error occurred when it tried to gate that register onto the A Bus.

The pattern is in the SA register.

④ The microdiagnostic transferred the contents of a good register into the failing register, but an error was not detected until it compared these two registers. This type of error would indicate that multiple bits are failing, for if only one bit failed a Check 1 should have occurred.

The pattern used is in the SA register.

⑤ The microdiagnostic was able to successfully set a pattern into the failing register. It was also able to gate that register onto the A Bus, but an error occurred when it tried to gate that register onto the B Bus.

The pattern used is in the SA register.

*Multiple Usage Card

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ROUTINE 82 - REGISTER TEST	BAR (Hex)	Check-1 Register bit 0	1	2	3	A Reg 4	B Reg 5	6	7	Error Description Failing Register	Possible Failing Replaceable Units
Register Tests Read additional information under "Additional Action and Reference Notes" on MICRO 405.	0578									TA register (4)	*A-B1E2, A-B2H2
	057C	0	X	X	X	1	0	X	X	GA register (3)	*A-B1E2
		0	X	X	X	0	1	X	X	TA register (5)	*A-B1E2
	0580									GA register (4)	*A-B1E2
	0584	0	X	X	X	0	1	X	X	ST register (5)	A-B2F2
	0588									ST register (4)	A-B2F2, A-B2M4
	058C	0	X	X	X	0	1	X	X	GD register (5)	*A-B1F2
	0590									GD register (4)	*A-B1F2
	0594	0	X	X	X	0	1	X	X	TG register (5)	A-B2F2
	0598									TG register (4)	A-B2F2
	059C	0	X	X	X	0	1	X	X	BR register (5)	A-B2F2
	05A0									BR register (4)	A-B2F2
	05A4	0	X	X	X	0	1	X	X	GE register (5)	*A-B1K2
	05A8									GE register (4)	*A-B1K2
	05AC	0	X	X	X	0	1	X	X	ME register (5)	*A-B1K2
	05B0									ME register (4)	*A-B1K2
	05B4	0	X	X	X	0	1	X	X	NE register (5)	*A-B1K2
	05B8									NE register (4)	*A-B1K2
	05BC	0	X	X	X	0	1	X	X	TE register (5)	*A-B1K2
	05C0									TE register (4)	*A-B1K2
	05FC									MA register (4)	A-B1Q2

Additional Action and Reference Notes

(3) The microdiagnostic was able to successfully set a pattern into the failing register, but an error occurred when it tried to gate that register onto the A Bus.

The pattern is in the SA register.

(4) The microdiagnostic transferred the contents of a good register into the failing register, but an error was not detected until it compared these two registers. This type of error would indicate that multiple bits are failing, for if only one bit failed a Check 1 should have occurred.

The pattern used is in the SA register.

(5) The microdiagnostic was able to successfully set a pattern into the failing register. It was also able to gate that register onto the A Bus, but an error occurred when it tried to gate that register onto the B Bus.

The pattern used is in the SA register.

*Multiple Usage Card

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (Special Ops and Checkers Routine 84)

1. Determine error code and message bytes on MICRO 25. *2. Refer to START 900-911 for data flow by card and common card information.*

Error Code (Hex)	Error Description	CE Panel Lamp Display		Possible Failing Replaceable Units	Additional Action and Reference Notes
		2ND BYTE	3RD BYTE		
8400				B2H2	
8401	Check 2 was on at entry to routine and will not reset.	Control Check conditions (NA Reg) Bit Meaning 0 Channel Buffer Parity Check 1 Interface Check – Chan A or C 2 Interface Check – Chan B or D 3 Data Transfer Check 4 CTL-I Check (defined by 3rd byte) 5 Load S – Registers Check 6 Compare Assist Check 7 Interface Check Chan C/D or Multiconnect	CTL-I check conditions (ND Reg) Bit Meaning 0 Controller Check 1 Select Active or Select Check 2 CTL-I Buffer Parity Error 3 Unexpected End Check 4 Tag Bus Parity Check 5 Bus Out Parity Check 6 CTL-I Transfer Error 7 Not Used	B1D2 B1Q2 A1R2 A1N2 A1M2 B2Q2	Special Op 03 (check reset) failed to reset the Check 2 error. If card replacement does not fix problem, refer to PANEL 50.
8402	Check 2 failed to set or Check 2 branch failed.			B1M2 B1B2 B1R2 A1T2 A1N2 B2Q2 B1U4	Error Alert (TB reg bit 2) was raised with both Select Hold and Select Active down. The resulting Select Active check should force Check 2. If card replacement does not fix problem, refer to PANEL 50 for second level of Check 2. (Check 2 branch is CH decode 11.)
8403	Check 2 did not reset after being turned on.			B1R2 B1M2	Special Op 03 (check reset) failed to reset the Check 2 error. If card replacement does not fix problem, refer to PANEL 50.
84xx				B2Q2 B2C2 B2B2 B2H2	

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1. Determine error code and message bytes on MICRO 25. *2. Refer to START 900-911 for data flow by card and common card information.*

Error Code (Hex)	Error Description	Expected BAR Pointer	Expected Check 1		Received BAR		Received Check 1		Possible Failing Replaceable Units	Additional Action and Reference Notes
		2ND BYTE (Hex)	3RD BYTE	4TH BYTE	5TH BYTE	6TH BYTE	7TH BYTE	8TH BYTE		
8405	Check 1 not as expected.	74							B2Q2 B2M2	A. If card replacement doesn't fix problem, refer to PANEL 40 for scope reference. Loop on error and use address '0574' as sync.
		78					'0000 0000' '0000 0000'	'0001 0000' '0010 0000'	B2P2 B2Q2 B2B2 B2C2 B3D2	B. Same as A above. Use '0578' as sync.
		A0							B2Q2 B2J2	C. Same as A above. Use '05A0' as sync.
		A4					'0000 0010' '0000 1000'	'0000 0000' '0000 0000'	B1H2 B2Q2 B1J2 B2Q2 B1N2	D. Same as A above. Use '05A4' as sync.
		A8					'0000 00x0' '0000 00x0' '0000 0xx0' '0000 0xx0'	'0x00 x000' '0x00 x000' '0000 x000' '0x00 0000'	B2Q2 (Bit 5 off) B1S2 B2Q2 (Bit 9 off) B2H2, B1H2 B2Q2 (Bit 12 off) B3U2 B1H2	E. Same as A above. Use '05A8' as sync. F. Will be caused by entering wrong control storage size at Hardcore stop '0800'. See START 25. G. If card B1G2 is present, the ECC jumper being plugged wrong on B1G2 can cause this error. See INST 20, step 6.
		B0							B2N2 B2Q2 B1U4	H. Same as A above. Use '05B0' as sync.
		B4							B2Q2 B2K2	I. Same as A above. Use '05B4' as sync.
		B8							B2Q2 B2K2	J. Same as A above. Use '05B8' as sync
		C0							B3T2 B2Q2 B2L2 A1S2	K. Same as A above. Use '05C0' as sync.
		F4							B2Q2 B2N2 B2M4 B2B2 B2C2 B1J2 B1N2 B1S2	L. If card replacement doesn't fix problem, refer to PANEL 40 for scope reference. Loop on error and use 05A0 as sync.

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (Special Ops and Checkers Routine 84)

1. Determine error code and message bytes on MICRO 25. *2. Refer to START 900-911 for data flow by card and common card information.*

Error Code (Hex)	Error Description	Expected BAR		CAS Address to Recycle	Possible Failing Replaceable Units	Additional Action and Reference Notes
		2ND BYTE (Hex)	3RD BYTE (Hex)			
8407	Failed to get Check 1.	05	74	05AC: K=128, A K→GA, D, C, B, F — Set up GA. 0574: A GA+GA→GAC, D, C 0→ST3C, B, F — Force CHK 1. More than 1 gate to ST3C.	B2Q2 B2M2 B2M4	This test must be run in forced logging mode; otherwise a Selective Reset and restart will not occur following the forced Check 1 errors. a. If card replacement does not fix problem, refer to PANEL 40 for scope reference to see why expected Check 1 (see error code 8405 for expected Check 1 message bytes) did not occur. Recycle addresses indicated at left, using Check Bypass for scope loop. Suspect trileads.
		05	78	05BC: A SPEC:04, D, C, B, F — Set diagnostic write latch. 0578: A 30(0)DAR, D, C STOR4, B, F — Force CHK 1. Store bad parity.	B1U4 B2Q2 B1S2 B2D2 B2E2	
		05	A0	05A0: A 0+TF→GC, D, C, B, F — Force CHK 1. TF reg nonexistent	B2Q2 B2J2	
		05	A4	05A4: A GC+0→ND, D, C, B, F — Force CHK 1. GC should have bad parity.	B2Q2	
		05	A8	05A8: 2, A 05(ND)→DAR, D, C FTCH4, B, F — Force CHK 1. ND should have bad parity.	B2Q2	
		05	B0	F: A SPEC:1F, D, C, B, F — Force CHK 1. Invalid special operation 31.	B2Q2 B1U4	
		05	B4	05B4: C, A 8000→IAR, D, C, B, F — Force CHK 1. Branch to invalid address.	B2Q2 B2K2	*Note: If Check 1 does not occur, machine hangs up in loop.*
		05	B8	05B8: C, A 4000→IAR, D, C, B, F — Force CHK 1. Branch to invalid address.	B2Q2 B2K2	*Note: Block is not tested on machines with over 4K of control storage. If Check 1 does not occur, machine hangs up in loop.*
		05	C0	05C0: A 30(0)→DAR, D, C, B, F — Force CHK 1. Word at '3000' should have bad parity.	B2Q2 B2L2	
		05	F4	05A0: A K=00100001 K+0→TF, D, C, B, F — Set up the TF Reg controls to force bad parity. 05F0: A SPEC:OC, D, C, B, F — Force bad parity in TF Reg. 05F4: A 0+TF→OC, D, C, B, F — Force CHK 1. GC should have Bad parity.	B2Q2 B2J2 B1G2	

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (CONTROL UNIT ROUTINE 86)

1. Match BAR indication with listing on these pages until a match is found. Take action indicated. 2. Refer to START 900-911 for data flow by card and common card information.

BAR (hex)	Error Description	CAS	FEALD	Possible Failing Replacealbe Units	Additional Action and Reference Notes
	ROUTINE 86 – ALU BRANCH TEST				
Display BAR on Stop ↓	Begin test with Operation Mode switch set to Forced Logging mode. There are no expected stops.				
0410	Test ALU AND function 'FF' is anded wtih '00'. Result should be '00'.		RA103, 104, RA203,204	Replace cards in the following order: 1. B1N2 2. B1H2 } Same part 3. B1J2 } number. May be swapped.	**Program Detected Error** When a stop occurs, perform the following: 1. Set Enter/Display switch to Program Data Entry/Display. Bits 8 through 15 specify the failing routine. 2. Set Enter/Display switch to BAR. Bits 0 through 15 are the instruction address of the stop or failing instruction. 3. Use the routine and the instruction address (BAR) to locate a failing unit. **Hardware Detected Error** Hardware detected errors cause the control unit to stop with the check-1 light turned on. 1. Set Enter/Display switch to Program Data Entry/Display. Bits 8 through 15 specify the failing routine. 2. Set Enter/Display switch to BAR. Bits 0 through 15 are the instruction address of the stop or failing instruction. Loop failure when possible. Check trilead and land patterns when card replacement does not resolve the problem. For all hardware detected check-1 errors, refer to Fault Symptom Index (begins on FSI 10). Refer to ALU check CTRL 60 and RA 303.
0418	Test ALU Exclusive OR function. '55' is exclusive ORed with '55'. Result should be '00'.		RA103, 104, RA203, 204		
0424 0428	Test of carry out and D bus = 0		RA302		
0430	Test ot carry and ST3C No Carry or ST3C		DE302		
0434 0438	No Carry No ST3C				
0440	With ST3C on, 'FF' is ANDed to '00', with carry in active. Result should be '00'.		RA303		
0470 0478	Test all bit OR function		RA103		
0480	Test no bit OR function		RA103		
0488	Test that '7E' + '01' + carry in = '80'		RA103		
0490	Test that 'FE' – 'FD' + no carry in = '00'.		RA303		
04F8 04FC	Test DNST21 statement in the test loop, leaves ST2 off			B2L2 B2M4	
0568	Test setting of each ST bit except ST4, by 1→ST bit statement		RB101, 102	B2L2	
0578	Test resetting of each ST bit except ST4, by 0 →ST bit statement		RB101, 102	B2L2	
05D4 05D8	All branch bits, all ST bits except ST1 and ST4 are set, reset and tested for proper branching. Display SD register to determine branching failure.		RB101, 103	If SD register = '34', '45', '66', replace B2L2. If SD register = '77', '88', '99', 'AA', replace B2F2 B2L2, B2S2, B1U4	

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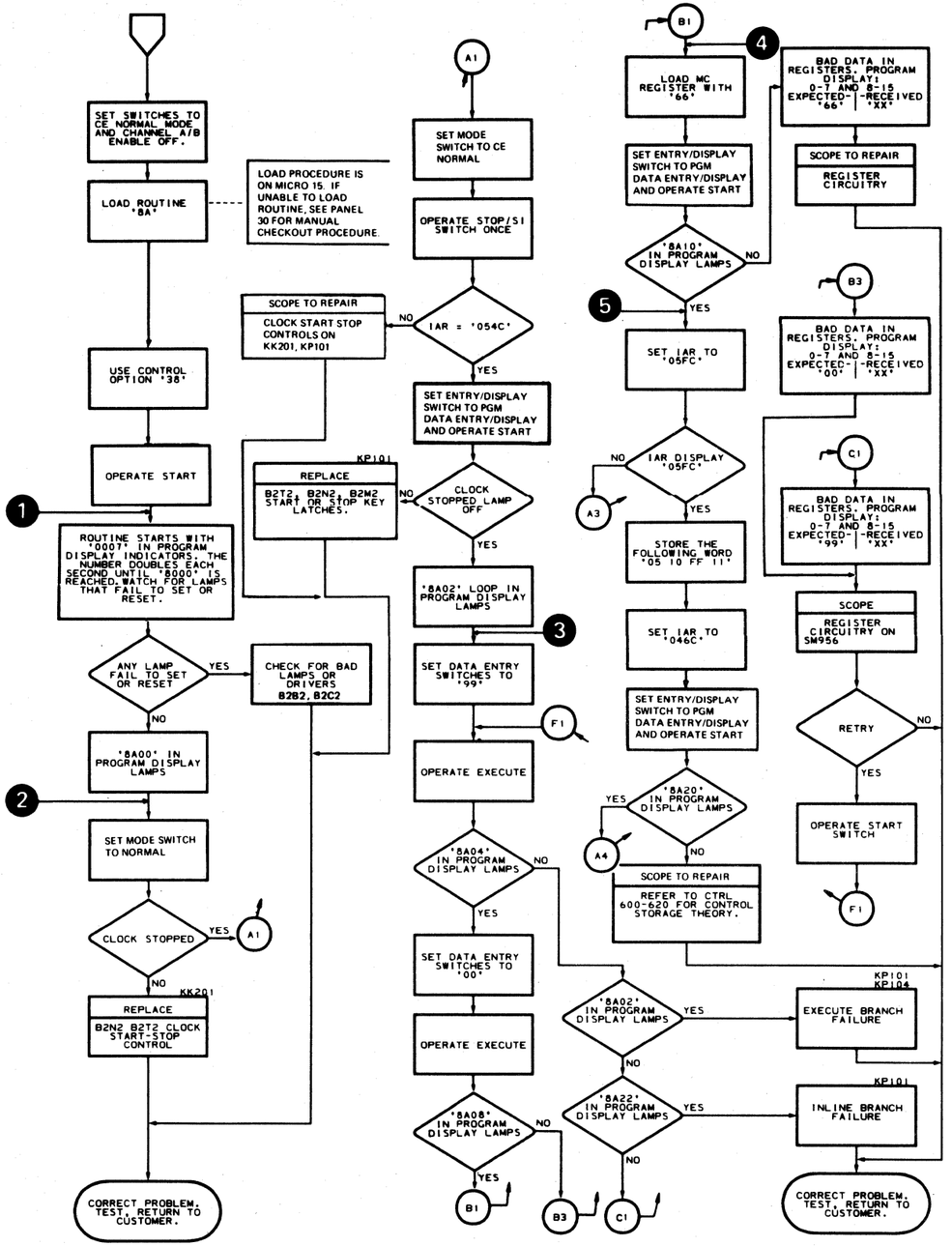
CE PANEL TEST

- Scope using FEALDs.



QUICK TEST CHART				For Single Function Testing and Midtest Entry
Flow Entry	Function Tested	IAR Set	Exit	Special Inst.
1	Lamps & drivers	0424	8A00 Display	SA=00 at start
2	Mode sw. & single cycle	0510	8A02 Display	
3	Data entry switches	0510	8A08 Display	
4	Manual reg. loading	0454	8A10 Display	
5	Addressing and storage alter	05FC	8A20 Display	
6	Recycle	058C	8A30 Display	ST7=0 at start
7	ACR stop	057C	05AC IAR	
8	Stop switch	05B4	05C4 IAR	
9	Micro reg. loading	05C0	8A60 Display	Match chart upon exit
10	Check-1	05E0	04A4 IAR	Ck-1 at exit
11	Check-2	04AC	04B0 IAR	Ck-2 at exit
12	Check Stop switch	04B8	8A80 Display	

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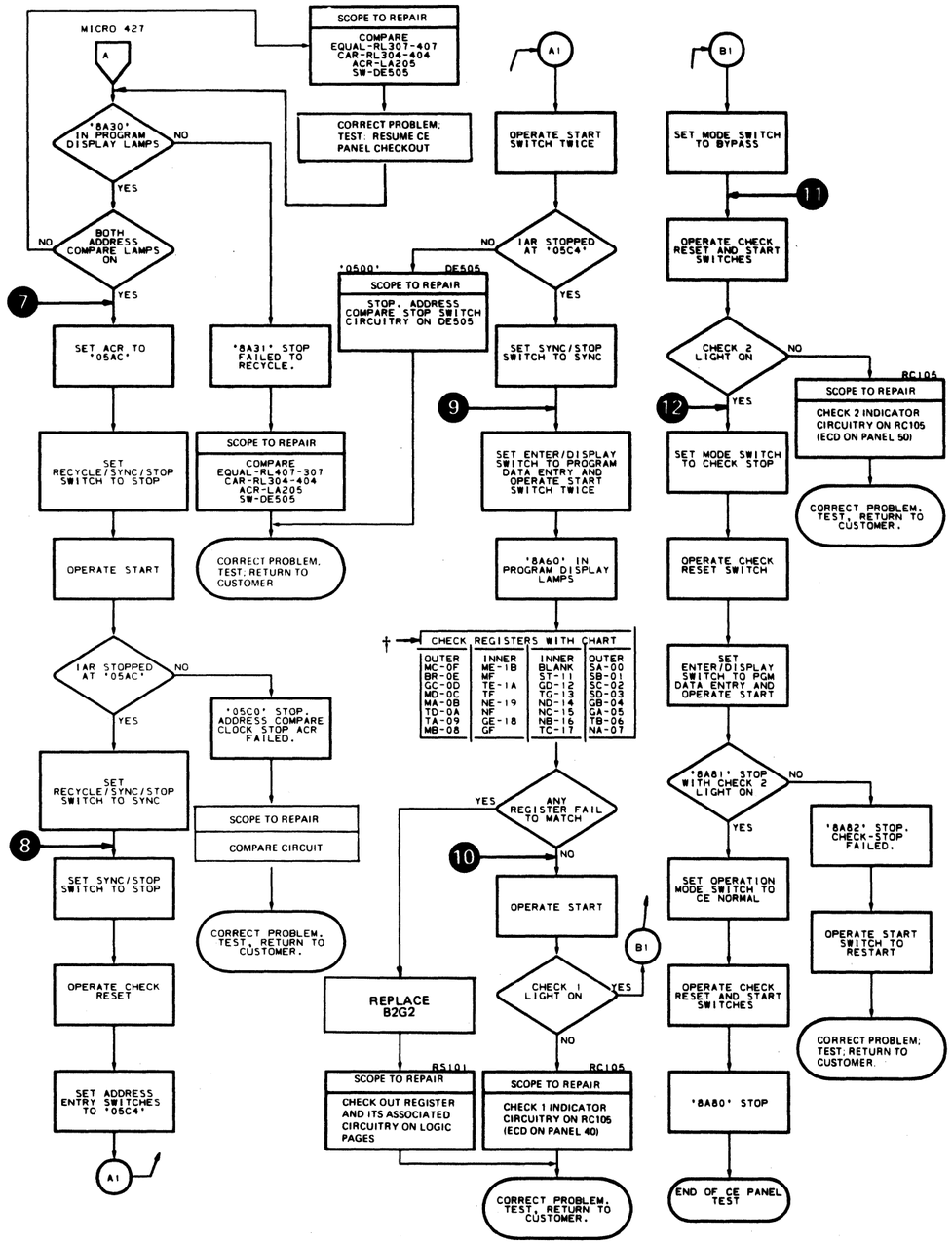
CONTROL UNIT ROUTINE 8A (Part 2 of 2)

CE PANEL TEST *(Continued)*



M12 10/12/72

† *E and F regs are optional with features.*
See INTR 005 for feature codes for these registers.

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1. *Match BAR indication with listing on these pages until a match is found. Take action indicated.*
2. *Refer to START 900-911 for data flow by card and common card information.*
3. *Refer to LGND section for logic symbology, voltage levels, etc.*

Error Code	Test No.	Error Description	CE Panel Lamp Display			Possible Failing Replaceable Units	Additional Action and Reference Notes
			2ND BYTE	3RD BYTE	4TH BYTE		
88——		This routine detects single or multi bit failures. Further parameter descriptions on MICRO 400.					For Check 1 error action other than storage errors refer to FSI 30. Refer to FSI 32, 33 for error analysis of storage errors and operating instructions.
88XX		With Halt On Error (3E) option selected the following error message is possible. XX = the failing bit or bits for the word under test.	High order portion of failing address.	Low order portion of failing address.	Failing byte (0, 1, 2, or 3)		Refer to FSI 32 and FSI 33.

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Error Code	2nd Byte	3rd Byte	4th Byte	Possible FRU	Error Description	Additional Action & Notes
96A1	TF Reg	GF-X was	GF-X S/B	A-B1G2	"GF-X" register addressing failure.	Each register has its address stored into it. All registers are checked to make sure each register contains its address. 2nd byte of error display is TF register with register address control. The 4th byte is the expected address value.
96A2	TF Reg	NF-X was	NF-X S/B	A-B1G2	"NF-X" register addressing failure.	
96A3	TF Reg	MF-X was	NF-X S/B	A-B1G2	"MF-X" register addressing failure.	
96C1	TF Reg	GF-0 was	00	A-B1G2	"GF-0" fetch should contain 0s, TF Reg is set up for semistep mode (C0).	Bit 0 of TF register = 1 allows the TF address register (Bits 3–7) to be step by instruction "0+MF→GC". Each register addressed will contain its address.
96C2	TF Reg	NF-0 was	00	A-B1G2	"NF-0" fetch should contain 0s, TF Reg is set up for semistep mode (C0).	
96C3	TF Reg	MF-0 was	00	A-B1G2	"MF-0" fetch should contain 0s. TF Reg is set up for semistep mode CB of MF should step TF Reg by 1".	
96C4	TF Reg	GF-X was	GF-X S/B	A-B1G2	"GF-X" selected, did not contain the address calculated for proper TF Reg operation.	The sequence of instructions is: 0+GF–X→GF, 0+NF–X→NF, & 0+MF→MF. The last instruction should step the TF address control 1 time each time it executes; GF, NF, and MF register contents are checked (should contain its address 01–1F).
96C5	TF Reg	NF-X was	NF-X S/B	A-B1-G2	"NF-X" selected did not contain the address calculated for proper TF Reg operation.	
96C6	TF Reg	MF-X was	MF-X S/B	A-B1-G2	"MF-X" select, did not contain the address calculated for proper TF Reg operation. CB and CD of MF should only step TF once.	
96C7	TF Reg	TF Reg	N/A	A-B1-G2	TF Register address control did not step back to 0 when last address was 1F and a step condition executed.	With TF register = DF, the execution of 0+MF→MF should step TF register to C0.
96C8	TF Reg	GF-0 was	GF-0 S/B	A-B1-G2	GF-X should contain its address. TF addr reg is stepped by CD of TA	Each time the instruction 0+GF→TA is executed, TF register is stepped once.
96C9	TF Reg	NF-0 was	NF-0 S/B	A-B1-G2	TF Reg was not stepped to C0 after being DF and a CD to TA was executed.	TF was DF and the instruction 0+NF→TA was executed.
96CA	TF Reg	MF-0 was	MF-0 FF	A-B1-G2	"D" bus contents were not stored into MF-0 when CD of TA was executed.	Each time CD of TA is executed, the D Bus should be stored into the selected MF register, controlled by the TF register.
96D1	TF Reg	GF-X was	GF-X S/B	A-B1G2	"GF-X" encountered an unexpected data word pattern.	Each register address is selected, set to 0's, and 1's added to it until the register is stepped back to zero. A check is made after adding each 1 into the selected register address. TF register indicates the selected register address.
96D2	TF Reg	NF-X was	NF-X S/B	A-B1G2	"NF-X" encountered an unexpected data word pattern.	
96D3	TF Reg	MF-X was	MF-X S/B	A-B1G2	"MF-X" encountered an unexpected data word pattern.	

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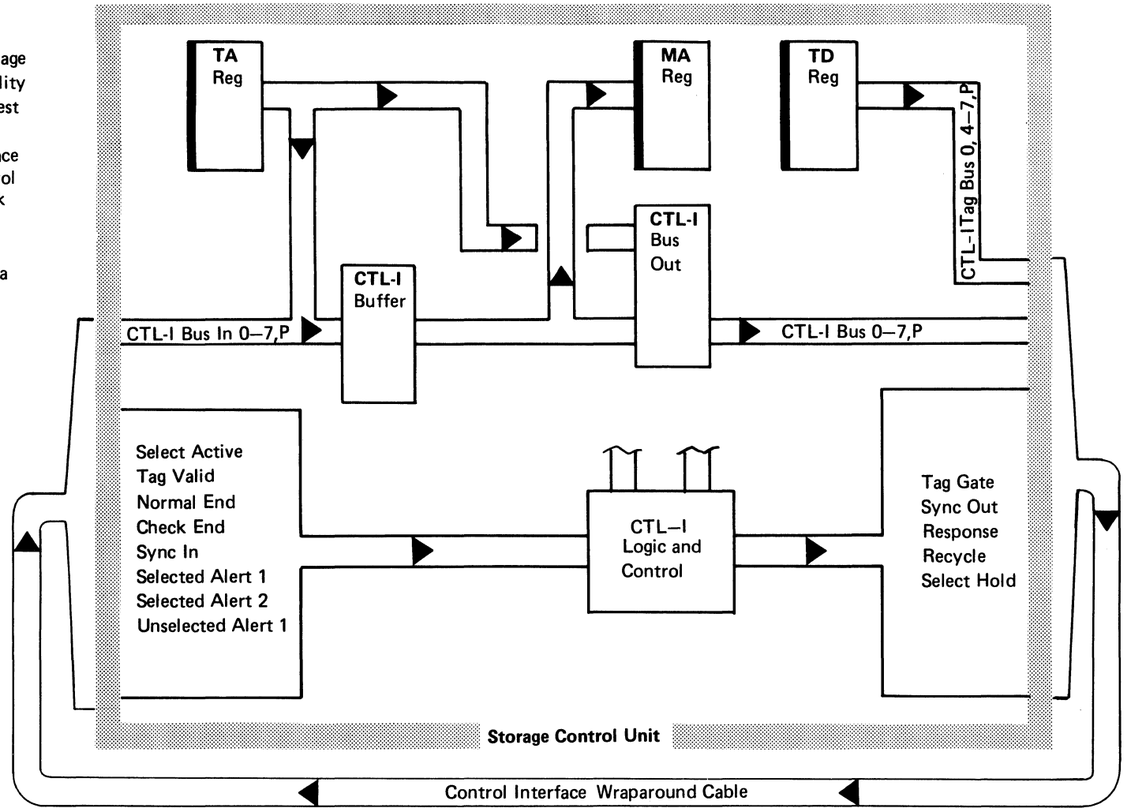
CONTROL INTERFACE (CTL-I) WRAPAROUND TEST

DESCRIPTION

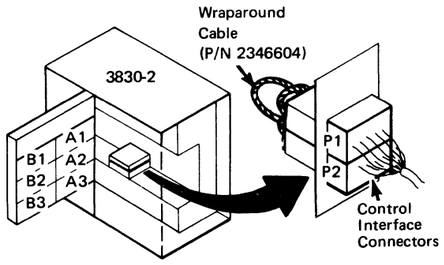
To verify that the control interface logic in the storage control unit is functioning properly and has the ability to transmit and receive data and control signals, a test cable and microdiagnostics are provided.
When connected, the cable takes the control interface outbound lines and loops them back into the control interface inbound lines. (See MICRO 506 for block diagram.)
Diagnostic routines 8C-94 exercise the control interface logic by raising outbound control and data lines and analyzing the returned inbound lines.
Detection of a failure is indicated by a check-1 or a normal error message. The Message Table on this page indicates the proper CE action.
The hardware tested includes:

- Control interface logic: locations B1B2, B1B4, B1C2, B1C4, B1D2, B1Q2, B1R2.
- Control unit logic associated with control interface: locations B1E2, B1F2, B1L2, B1M2, B1P2, B1U4, B2D2, B2E2, B2F2, B2L2, B2M4.
- Control interface cables and connectors.



RUNNING INSTRUCTIONS

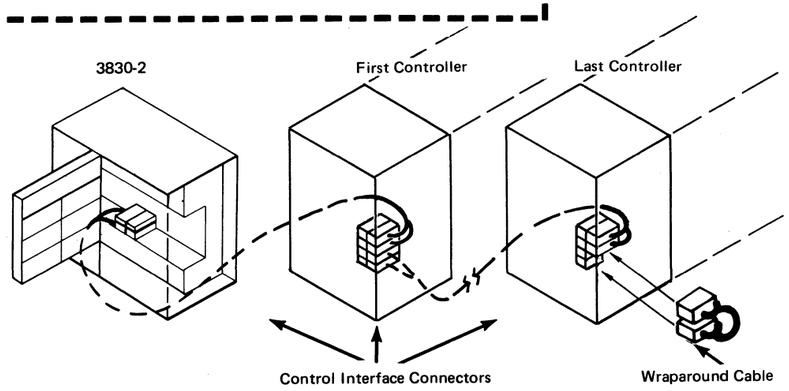
1. Disable channel interfaces.
2. Install control interface wraparound cable in 3830-2 as shown below.



3. Set Operation Mode switch to CE Normal.
4. Set Enter/Display switch to Program Data Entry/Display.
5. Set Data Entry switches to '8C'.
6. Operate Execute switch.
7. Set Data Entry switches to '38'.
8. Operate Execute switch. The control interface tests will begin to run and will continue until all tests are complete or an error is found. If normal completion display of 'C494' is not received, see Message Table for action.
9. If all tests run successfully with the wraparound cable installed in the 3830-2, the interface cables and data path through the controller may be tested by attaching the wraparound cable in the last controller as shown at right.

   Note: *Since the wrap test effectively doubles the length of the control Interface cable, it is recommended that the cable length from the storage control to the last controller does not exceed 150 feet. Greater cable length could result in marginal test results due to the line and connector attenuation.*

   Remove terminators (see device MLM for location); then install control interface wraparound cable in their place. Power off all controllers; then rerun diagnostic routines 8C-94.



Message Table

CE Panel Indication	Description
–Program Display Lamps– 1000 1111 xxxx xxxx	Tests is running; no errors have been found. If clock stopped, see below.
1100 0100 1001 0100	Test has completed with no errors.
1000 0001 xxxx xxxx (For any other display, see MICRO 16.)	Test has found an error; 1. Determine error code (MICRO 25). 2. Use error code to enter error code dictionary (begins on MICRO 515).
Other Indicators	**Description**
Clock Stopped, Check 2.	Test forces check-2 errors. Do not run in check-stop mode.
Clock Stopped, Check 1.	Record IAR and BAR. Compare with listings in Control Interface Check-1 Analysis Dictionary (begins on MICRO 800). If no match is found, see FSI 30-55 to analyze failure.

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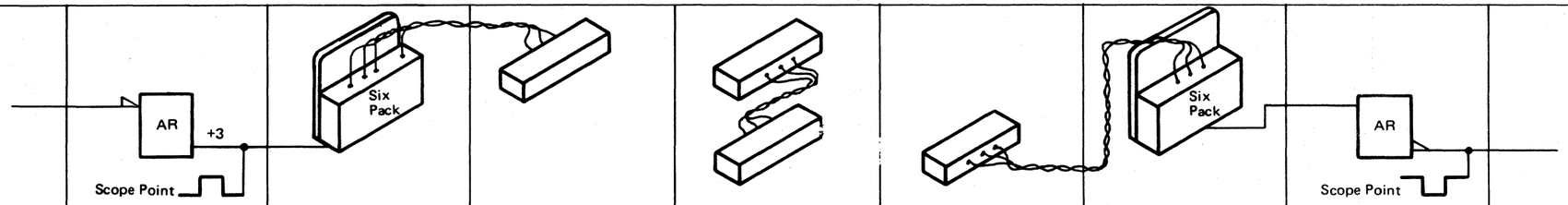
CONTROL INTERFACE WRAPAROUND TEST (SCOPE POINTS AND CABLE DIAGRAM)



CI OUTBOUND LINE NAME	DRIVER	LEAVES BOARD	LEAVES CONNECTOR	WRAPAROUND CABLE	ENTERS CONNECTOR	ENTERS BOARD	RECEIVER	CI INBOUND LINE NAME
BUS OUT 0	B1B2B09	B1A4B04	BUS D04	→	BUS J04	B1A4D04	B1C2J13	BUS IN 0
BUS OUT 1	B1B2B05	B1A4B05	BUS B05	→	BUS G05	B1A4D05	B1C2D09	BUS IN 1
BUS OUT 2	B1B2B10	B1A4B06	BUS D06	→	BUS J06	B1A4D06	B1C2G12	BUS IN 2
BUS OUT 3	B1B2B07	B1A4B07	BUS B08	→	BUS G08	B1A4D07	B1C2D04	BUS IN 3
BUS OUT 4	B1B2D10	B1A4B09	BUS D09	→	BUS J09	B1A4D09	B1C2J12	BUS IN 4
BUS OUT 5	B1B2D11	B1A4B10	BUS B10	→	BUS G10	B1A4D10	B1C2D06	BUS IN 5
BUS OUT 6	B1B4B09	B1A4B11	BUS D11	→	BUS J11	B1A4D11	B1B2J13	BUS IN 6
BUS OUT 7	B1B4B05	B1A4B12	BUS B12	→	BUS G12	B1A4D12	B1B2D09	BUS IN 7
BUS OUT P	B1B4B10	B1A4B03	BUS B03	→	BUS G03	B1A4D03	B1B2G12	BUS IN P
TAG BUS 0	B1C2B09	B1A3B03	TAG B03	→	TAG G03	B1A3D03	B1B2J12	SELECT ACTIVE
TAG BUS 4	B1C2B05	B1A3B05	TAG B05	→	TAG J04	B1A3D04	B1B2D06	TAG VALID
TAG BUS 5	B1C2B10	B1A3B04	TAG D04	→	TAG G05	B1A3D05	B1C4J13	NORMAL END
TAG BUS 6	B1C2B07	B1A3B07	TAG B08	→	TAG J06	B1A3D06	B1C4D09	CHECK END
TAG BUS 7	B1C2D10	B1A3B06	TAG D06	→	BUS J13	B1A4D13	B1B2D04	SYNC IN
TAG BUS P	B1C2D11	B1A3B09	TAG D09					
TAG GATE	B1C4B05	B1A3B10	TAG B10	→	TAG G08	B1A3D07	B1C4G12	SELECTED ALERT 1
SYNC OUT	B1C4B07	B1A4B13	BUS D13	→	TAG J09	B1A3D09	B1C4D04	SELECTED ALERT 2
RESPONSE	B1C4B10	B1A3B12	TAG B12					
RECYCLE	B1C4D10	B1A3B13	TAG D13					
SELECT HOLD	B1C4B09	B1A3B11	TAG D11	→	TAG G12	B1A3D12	B1B4J13	UNSELECTED ALERT 1

This chart is to be used with Control interface wrap-around tests 8C-94.

If one of the microdiagnostics stops with an error code which indicates that a signal was placed on an outbound line and its return was not received on an inbound line, use this diagram to locate the failing unit.

Example:

Microdiagnostic error code 8E5A (Tag bus 4 turned on but tag valid not received).

If suggested card swaps or replacements do not correct the problem, scope the output driver (B1C2B05) and the input receiver (B1B2D6) while recycling CAS shown in error code dictionary.

If the signal is present at the driver but missing at the receiver, unplug the output six pack (B1A3B5) and the input six pack (B1A3D4). Then check the continuity of the cables to find the point of failure.

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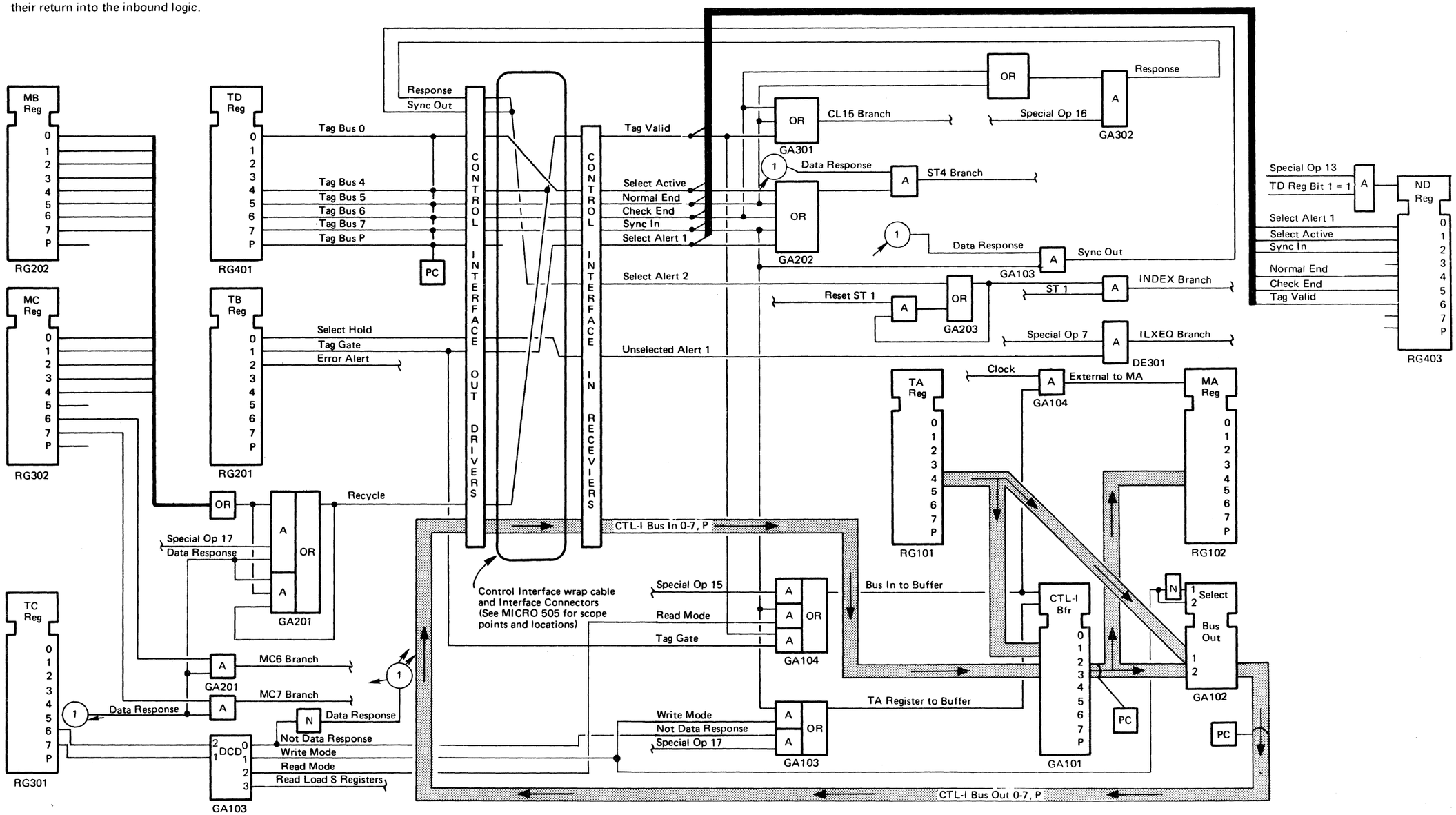
CONTROL INTERFACE LOGIC WITH WRAPAROUND CABLE INSTALLED

This diagram represents the Control Interface logic with the CTL-I wrap cable installed. It should be used for reference when running the CTL-I microdiagnostics (8C–94).

The Control Interface tests raise outbound lines, then test for their return into the inbound logic.

This diagram is intended for instruction only.
Use machine logics for troubleshooting and scoping.



AU5350	2347372
Seq 1 of 1	Part Number

437404	437405	437408	437414	437415		
23 Jun 72	15 Aug 72	16 Oct 72	4 Jun 73	2 Nov 73		

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CONTROL INTERFACE WRAPAROUND ROUTINE SUMMARY

Microdiagnostic Routines	Operating Mode: STAND-ALONE	Operating Mode: INLINE	Operating Mode: ONLINE	Control Options	Parameter Entries	Comments
8C Tests: 1. MC6 and MC7 branch 2. Data Response decode 3. Load S register logic **8E** Tests: 1. Compare assist logic 2. Tag bus 3. Selected Alert 1 4. Select Active 5. Sync In 6. Normal End 7. Check End 8. Tag Valid **90** Tests: 1. Recycle 2. CL15 branch 3. Select check **92** Tests: 1. ST4 branch 2. Controller check 3. Transfer check 4. CTL-I buffer 5. Bus out/bus in **94** Tests: 1. Select Hold 2. Unselected Alert 1 3. Selected Alert 2 4. Index 5. Response 6. Sync Out	Yes	No	No	Loop Options: 02 Bypass Loop Count 04 Inhibit Link 32 Loop Program Error Control: 01 Continue on Error 3E Halt on Error	None	See MICRO 500 before running tests **8C - 94**. Tests must be run in CE Normal mode. For additional information, see MICRO 500, 505, 506, CTL-I section, MICRO 515 (Error Code Dictionary), FEALDS GA101-GA709

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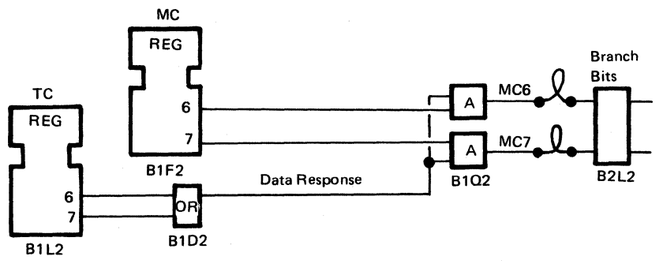
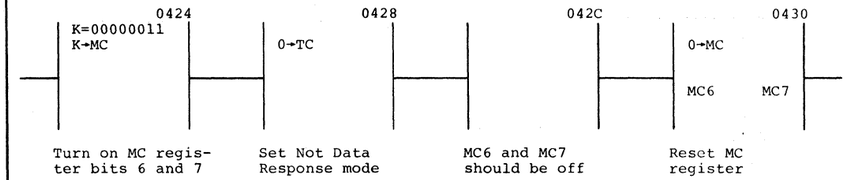
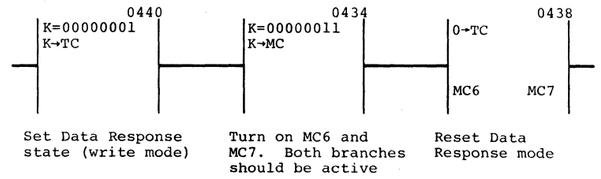
Match error code with listing on these pages.
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8C08	B1D2 Data Response Decode B1Q2 MC6 and MC7 Gating B1L2 TC Register (Swap with B1F2)	**Hot Gate to MC6 and MC7 branch.** MC register bits 6 and 7 were turned on, then the CTL-I logic was set to Not Data Response mode by turning off TC register bits 6 and 7. Not Data Response should have degated MC6 and MC7, but when sampled they were found active. 	GA201 Gate to MC6 and MC7	0424-0430	
8C0A	B1L2 TC Register (Swap with B1F2) B1D2 Data Response Decode	**Data Response state not set when TC register = 01.** TC register bit 7 was turned on, which should have set Data Response mode. Data Response was tested by branching on MC6 and MC7. The branch was successful for Read mode (TC register = 02), but not for Write mode (TC register = 01).	GA103 Data Response Decode GA201 Gate to MC6 and MC7	0440-0438	

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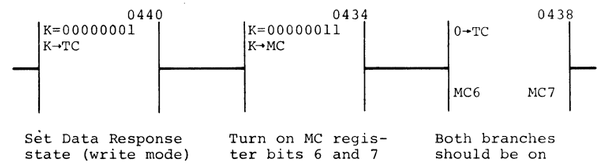
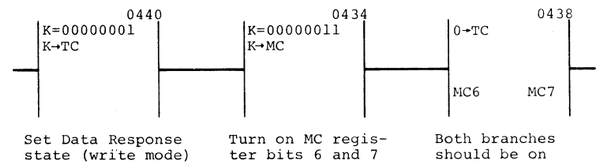
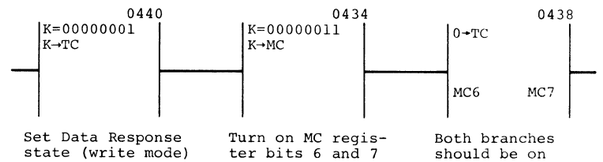
MICRODIAGNOSTIC ERROR CODE DICTIONARY (Control Interface Wraparound)

Match error code with listing on these pages.
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8C0C	B1D2 Data Response Decode B1Q2 MC6 and MC7 Gating	**Missing gate for MC6 and MC7 branch.** MC register bits 6 and 7 were turned on, then the CTL-I logic was set to Data Response mode by turning on TC register bit 7 (write mode). Data Response should have gated MC6 and MC7, but when tested they were found inactive.	GA201 MC6 and MC7 gate	0440-0438	
8C0E	B1Q2 Logic MC6 B1L2 MC Register (Swap with B1F2)	**MC6 branch not on.** MC register bits 6 and 7 were turned on with the CTL-I logic in Data Response mode. A test branch was made and MC6 branch was off.	GA201 Logic MC6	0440-0438	
8C10	B1Q2 MC7 Logic B1L2 MC Register (Swap with B1F2)	**MC7 branch not on.** MC register bits 6 and 7 were turned on with the CTL-I logic in Data Response mode. A test branch was made and the MC7 branch was off.	GA201 MC7 Logic	0440-0438	

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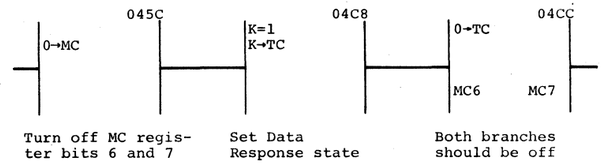
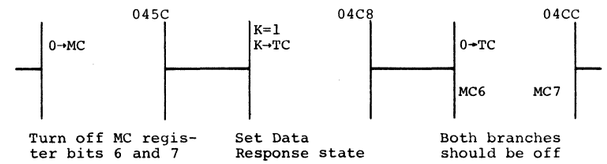
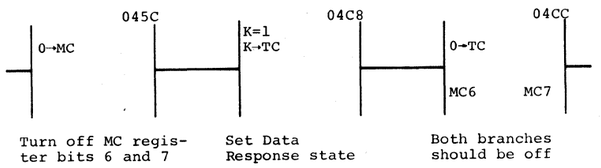
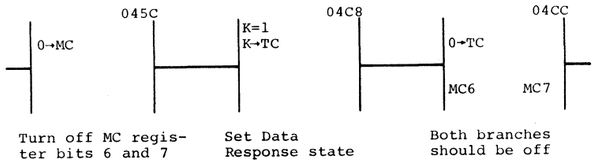
Match error code with listing on these pages.
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8C12	B1Q2 MC7 Gate B2L2 MC7 Branch Tri-Lead (See GA201 for location)	**Hot MC7 branch.** MC register bits 6 and 7 were turned off. When tested, the MC7 branch was on.	DE306 MC7 (CL 11) Branch	045C-04CC	
8C14	B1Q2 MC7 Gate B1L2 MC Register (Swap with B1F2)	**Hot input to MC7 branch.** MC register bits 6 and 7 were turned off. When tested, the MC7 branch was on.	GA201 MC7 Gate	045C-04CC	
8C16	B1Q2 MC6 Gate B2L2 MC6 Branch Tri-Lead (See GA201 for location)	**Hot MC6 branch.** MC register bits 6 and 7 were turned off. When tested, the MC6 branch was on.	DE306 MC6 (CH 13) Branch	045C-04CC	
8C18	B1Q2 MC6 Gate B1L2 MC Register (Swap with B1F2)	**Hot input to MC6 branch.** MC register bits 6 and 7 were turned off. When tested, the MC6 branch was on.	GA201 MC6 Gate	045C-04CC	

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (Control Interface Wraparound)

Match error code with listing on these pages.
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8C1A	B1D2 Data Response Decode B1L2 TC Register (Swap with B1F2)	**Data Response mode not set when TC register = 02.** TC register bit 6 was turned on, which should have set Data Response state. Data Response was tested by branching on MC6. The branch was successful for Write mode (TC register = 01) but not for Read mode (TC register = 02).	GA103 Data Response Decode	0490-04E4	0490: K=00000010 K→TC — Set Data Response state (read mode) 04E0: K=00000010 K→TC — Turn on MC register bit 6 04E4: 0→TC MC6 — Branch should be active
8C1C	B1D2 Data Response Decode	**Data Response mode not set when TC register = 03.** TC register bits 6 and 7 were turned on, which should have set Data Response mode. Data Response was tested by branching on MC6. The branch was successful for Read mode (TC register = 02) but not for Read Load S Register mode (TC register = 03).	GA103 Data Response Decode	04B8-04D8	04B8: K=00000011 K→TC — Set Data Response state (Read Load S Registers) 04D4: K=00000010 K→MC — Turn on MC register bit 6 04D8: 0→TC MC6 — Branch should be active

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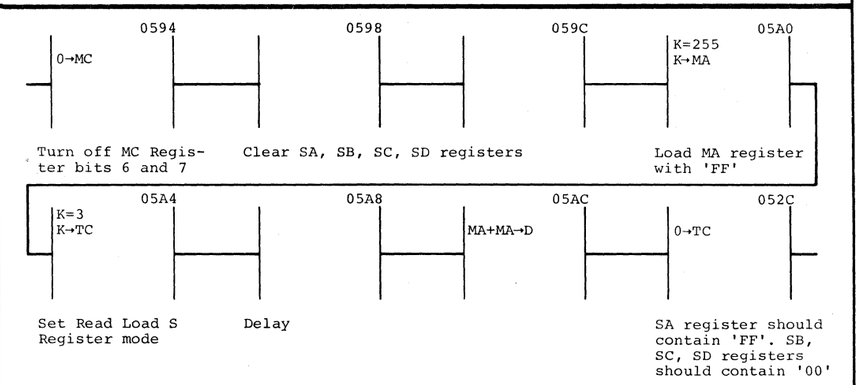
Match error code with listing on these pages.
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8C20	B1Q2 Load S Register Logic B2D2 SA Register (Swap with B2E2) B2S2 External Gates to S Registers B1D2 Load S Register Decode	**Load S register failure.** (See CTL-I 190 for description of Load S Register logic.) The Control Interface logic was set to Read, Load the S Registers mode (TC register = 03), then the microword MA+MA→D was executed. This should have caused the MA register to be gated into the SA register. When tested, the SA register was not equal to the MA register. MC register bits 6 and 7 determine which S register the MA register should be gated into. In this case, both bits were off, which selects the SA register. The error message contains the contents of the S registers at the time of failure. **Byte 1**: Error Code (20) **Byte 2**: N/A **Byte 3**: N/A **Byte 4**: N/A **Byte 5**: SA Reg **Byte 6**: SB Reg **Byte 7**: SC Reg **Byte 8**: SD Reg **Byte 9**: Routine Number (8C)	GA202 Load S Register Logic RS101 SA Register LA202 External Gates to S Registers	0594-052C	 *Note: Adjust time per division until Sync pulse touches both sides of the scope screen. See GA202 for scope points.*
8C22	B1Q2 Load S Register Logic	**Multiple S registers loaded.** The operation described for error code 8C20 was performed successfully. The MA register was gated into the SA register but it was also gated into one or more of the other S registers. Recycle the microwords shown for error 8C20, then scope the external gates to the S registers.	GA202 Load S Register Logic		Same as shown for error code 8C20

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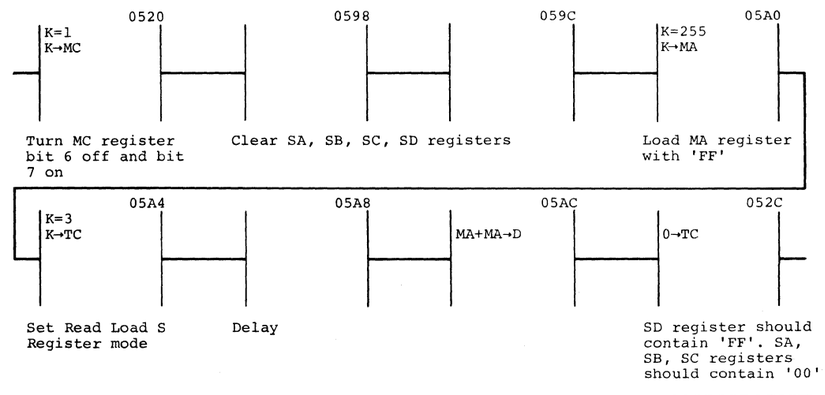
MICRODIAGNOSTIC ERROR CODE DICTIONARY (Control Interface Wraparound)

Match error code with listing on these pages.
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8C24	B1Q2 Load S Register Logic B2E2 SD Register (Swap with B2D2) B2S2 External Gates to S Registers	**Load S register failure.** (See CTL-I 190 for description of Load S Register logic.) The Control Interface logic was set to Read, Load the S Registers mode (TC register = 03), then the microword MA+MA→D was executed. This should have caused the MA register to be gated into the SD register. When tested, the SD register was not equal to the MA register. MC register bits 6 and 7 determine which S register the MA register should be gated into. In this case, bit 6 is off and bit 7 is on, which selects the SD register. The error message contains the contents of the S registers at the time of failure. **Byte 1**: Error Code (24) **Byte 2**: N/A **Byte 3**: N/A **Byte 4**: N/A **Byte 5**: SA Reg **Byte 6**: SB Reg **Byte 7**: SC Reg **Byte 8**: SD Reg **Byte 9**: Routine Number (8C)	GA202 Load S Register Logic RS201 SD Register LA202 External Gates to S Registers	0520-052C	 *Note: Adjust time per division until Sync pulse touches both sides of the scope screen. See GA202 for scope points.*
8C26	B1Q2 Load S Register Logic	**Multiple S registers loaded.** The operation described for error code 8C24 was performed successfully. The MA register was gated into the SD register, but it was also gated into one or more of the other S registers. Recycle the microwords shown for error 8C24, then scope the external gates to the S registers.	GA202 Load S Register Logic	0520-052C	Same as shown for error code 8C24

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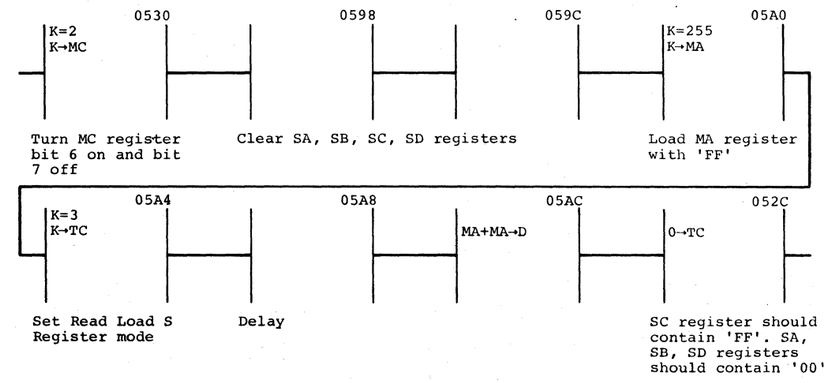
Match error code with listing on these pages.
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8C28	B1Q2 Load S Register Logic B2D2 SC Register (Swap with B2E2) B2S2 External Gates to S Registers	**Load S register failure.** (See CTL-I 190 for description of Load S Register logic.) The Control Interface logic was set to Read, Load the S Registers mode (TC register = 03), then the microword MA+MA>D was executed. This should have caused the MA register to be gated into the SC register. When tested, the SC register was not equal to the MA register. MC register bits 6 and 7 determine which S register the MA register should be gated into. In this case, bit 6 is on and bit 7 is off, which selects the SC register. The error message contains the contents of the S registers at the time of failure. **Byte 1** Error Code (28) — **Byte 2** N/A — **Byte 3** N/A — **Byte 4** N/A — **Byte 5** SA Reg — **Byte 6** SB Reg — **Byte 7** SC Reg — **Byte 8** SD Reg — **Byte 9** Routine Number (8C)	GA202 Load S Register Logic RS103 SC Register LA202 External Gates to S Registers	0530-052C	 *Note: Adjust time per division until Sync pulse touches both sides of the scope screen. See GA202 for scope points.*
8C2A	B1Q2 Load S Register Logic	**Multiple S registers loaded.** The operation described for error code 8C28 was performed successfully. The MA register was gated into the SC register, but it was also gated into one or more of the other S registers. Recycle the microwords shown for error 8C28, then scope the external gates to the S registers.	GA202 Load S Register Logic	0530-052C	Same as shown for error code 8C28

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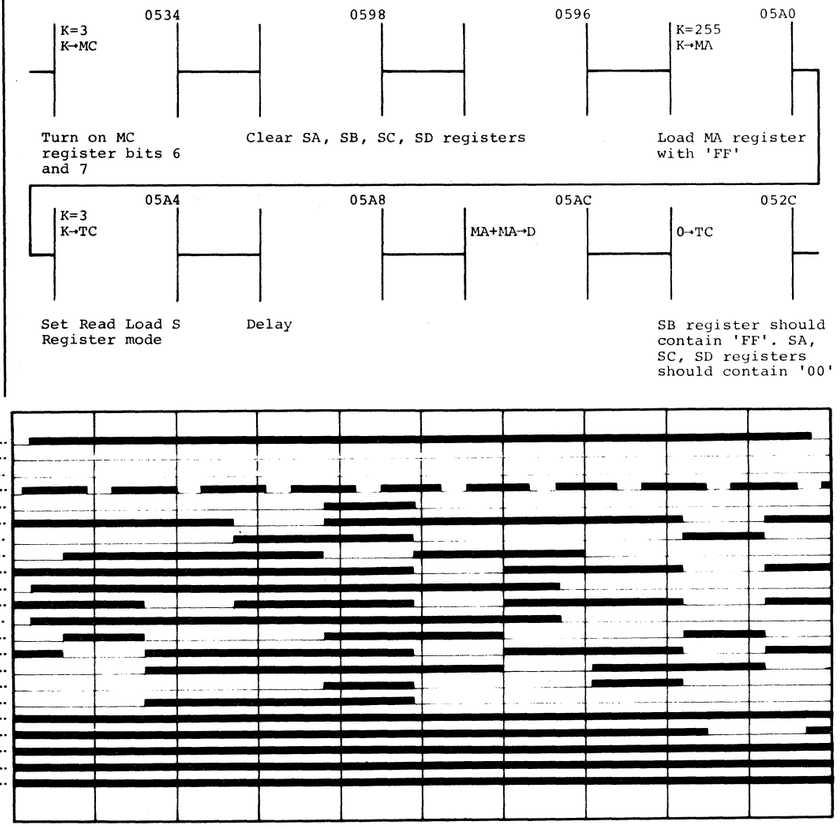
MICRODIAGNOSTIC ERROR CODE DICTIONARY (Control Interface Wraparound)

Match error code with listing on these pages.
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8C2C	B1Q2 Load S Register Logic B2E2 SB Register (Swap with B2D2) B2S2 External Gates to S Registers	**Load S register failure.** (See CTL-I 190 for description of Load S Register logic.) The Control Interface logic was set to Read, Load the S Registers mode (TC register = 03), then the microword MA+MA→D was executed. This should have caused the MA register to be gated into the SB register. When tested, the SB register was not equal to the MA register. MC register bits 6 and 7 determine which S register the MA register should be gated into. In this case, both bits were on, which selects the SB register. The error message contains the contents of the S registers at the time of failure. **Byte 1**: Error Code (2C) **Byte 2**: N/A **Byte 3**: N/A **Byte 4**: N/A **Byte 5**: SA Reg **Byte 6**: SB Reg **Byte 7**: SC Reg **Byte 8**: SD Reg **Byte 9**: Routine Number (8C)	GA202 Load S Register Logic RS203 SB Register LA202 External Gates to S Registers	0534-052C	 *Note: Adjust time per division until Sync pulse touches both sides of the scope screen. See GA202 for scope points.*
8C2E	B1Q2 Load S Register Logic	**Multiple S registers loaded.** The operation described for error code 8C20 was performed successfully. The MA register was gated into the SB register, but it was also gated into one or more of the other S registers. Recycle the microwords shown for error 8C2C, then scope the external gates to the S registers.	GA202 Load S Register Logic	0534-052C	Same as shown for error code 8C2C

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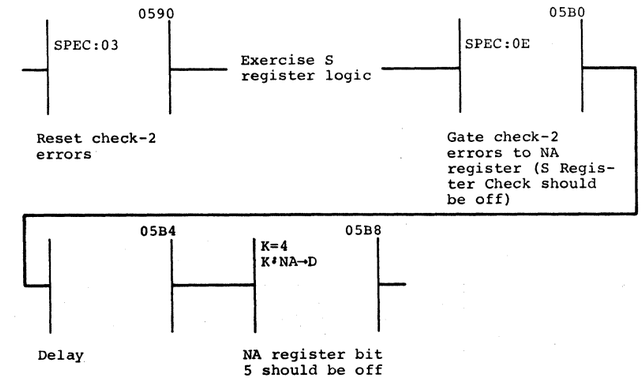
Match error code with listing on these pages.
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8C30	B1Q2 Load S Register Checker	**Defective Load S Register Checker.** The Load S Register logic was exercised and found to function properly. Then special operation 14 was executed, which gates check-2 errors into the NA register. When the NA register was examined, bit 5 (Load S Register Check) was on.	GA202 Load S Register Checker GK602 Assembler for External Inputs to NA Register	0590-05B8	

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (Control Interface Wraparound)

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Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8E32	B1M2 MB Register (Swap with B1F2) B1Q2 Gate B1P2 CD Decode B1U4 Op 24	**External gate to MB register failed.** The MB register was loaded with 'FF', then Special Op 24 was performed, which should have gated the compare assist latches to MB register bits 0 and 1, and 0s to MB register bits 2 through 7. After special Op 24 the MB register was tested and it still contained 'FF'.	RG202 MB register	044C-0418	044C 04A4 0418 K=255 K→MB SPEC:24 Load MB register with 'FF' Gate external to MB register MB register should contain '00'
8E34	B1M2 MB Register (Swap with B1F2)	**MB register bits 2 through 7 not all reset.** The MB register was loaded with 'FF', then Special Op 24 was performed, which should have gated 0s to MB register bits 2-7. After Special Op 24 the MB register was tested and bits 2 through 7 were not all 0s.	RG202 MB register	044C-0418	044C 04A4 0418 K=255 K→MB SPEC:24 Load MB register with 'FF' Gate external to MB register MB register should contain '00'
8E36	B1Q2 Compare Assist Latches B1M2 MB Register (Swap with B1F2)	**Hot compare assist latch.** The MB register was loaded with 'FF'. Then Special Op 24, which gates the compare assist latches to MB register bits 0 and 1, was performed. Both latches should have been off at this time. After Special Op 24 the MB Register was tested and one or more of the bits was on.	RG202 MB register GA203 Compare assist logic	044C-0418	044C 04A4 0418 K=255 K→MB SPEC:24 Load MB register with 'FF' Gate external to MB register MB register should contain '00'

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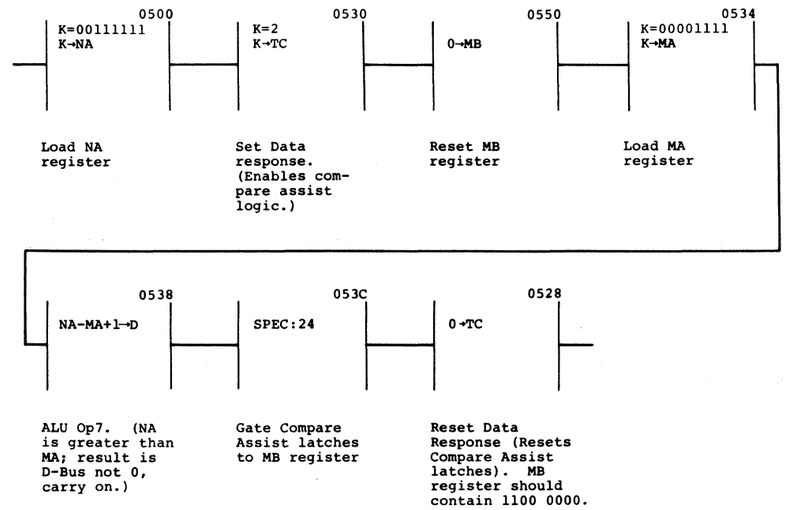
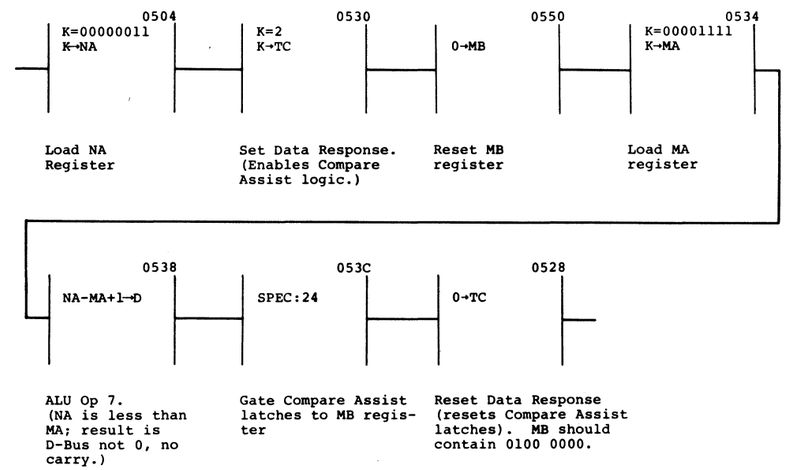
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8E40	B1Q2 Compare Assist Logic B2N2 Clock	**Compare assist failure.** An ALU Op 7 was performed. It resulted in a D-bus not zero condition with a carry. The CTL-I logic was in the Data Response mode, so the compare assist latches (D-Bus Not Zero and Carry) should both have latched up. The latches were gated by Spec Op 24 to MB register bits 0 and 1 for checking. Both bits should have been on.	GA203 Compare assist logic RG202 MB register	0500-0528	
8E41	B1Q2 Compare Assist Logic	**Compare assist failure.** An ALU Op 7 was performed. It resulted in a D-Bus not zero condition with no carry. The CTL-I logic was in the Data Response mode, so the compare assist latch D-Bus Not Zero should have latched up, and the Carry latch should have remained reset. The latches were checked by using Special Op 24 to gate them into MB register bits 0 and 1. Bit 0 should have been off; bit 1 should have been on.	GA203 Compare assist logic RG202 MB register	0504-0528	

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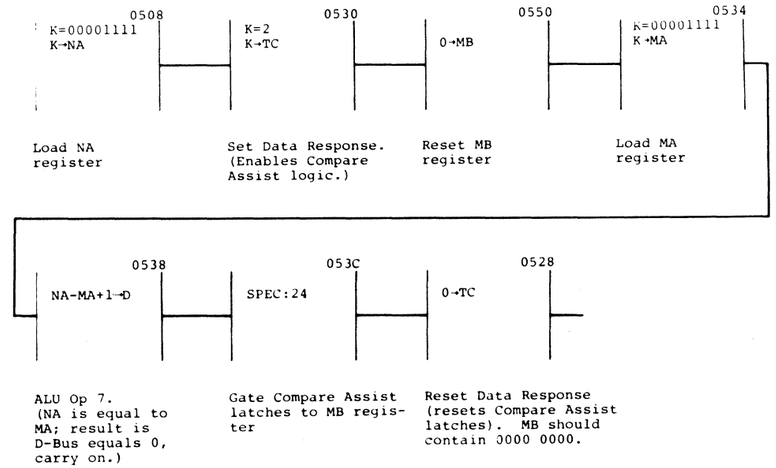
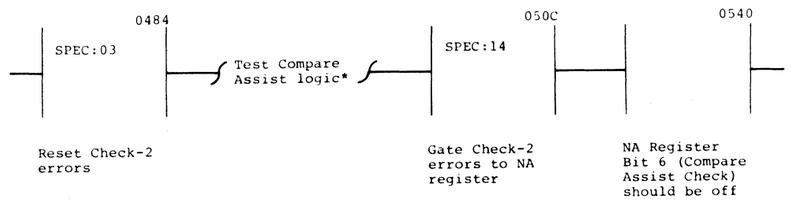
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8E42	B1Q2 Compare Assist Logic B2N2 Clock	**Compare assist failure.** An ALU Op 7 was performed. It resulted in a D-Bus equal zero condition with a carry. The CTL-I logic was in the data response mode, so the compare assist latch Carry should have latched up and the D-Bus Not Zero latch should have remained reset. The latches were examined by using Special Op 24 to gate them into MB register bits 0 and 1. Both bits should have been off. Note: The Carry bit is degated by the D-Bus equal zero condition.	GA203 Compare assist logic RG202 MB register	0508-0528	
8E43	B1Q2 Compare Assist Logic A1T2	**Compare assist logic check circuit failure.** The compare assist logic was exercised * and found to function properly. After the test, Special Op 14 was performed, which gates Check 2 errors into the NA register. When examined, NA register Bit 6 (Compare Assist Check) was on. * See error codes 8E40, 8E41, and 8E42 for CAS and description of the tests that were performed. Individual tests may be looped but there is no Special Op 03 to reset the Compare Assist Check latch once it is set.	GA203 Compare assist logic	0484-0540	

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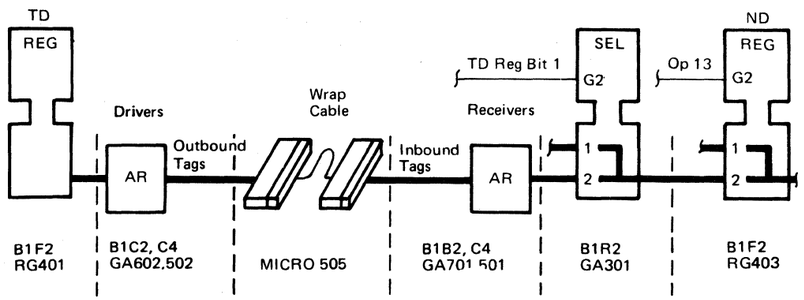
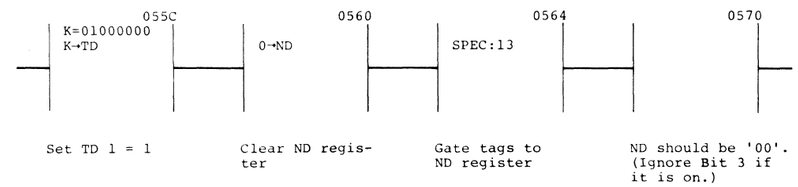
Match error code with listing on these pages.
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8E46	See tables on this page	**Hot control interface tag.** The CTL-I inbound tags have a path to the ND register. The tags were gated into ND by a Special Op 13 with TD register bit 1=1. All tags should have been inactive but were not. The second error message byte contains the contents of the ND reg after Special Op 13. With the wrap cable installed, a hot outbound tag will be returned by the cable and appear to be a hot inbound line. (See MICRO 505 for outbound-to-inbound conversion.) To determine whether the failure is outbound or inbound, remove the tag end of the wrap cable and rerun test 8E. If this error occurs with cable disconnected, the failure is inbound. If error 8E48 occurs, failure is outbound. Determine the possible failing units by matching any bit that is on in the second message byte and failure mode with tables on this page.  To Scope: Reinstall the wrap cable; then recycle the words shown. Scope inbound failures at the input to the ND register. Scope outbound failures at their drivers.	See tables	055C-0570	

Hot Inbound Line (error code **8E46** with cable connected or disconnected)

Message Byte 2	Hot Inbound Line	Probable Failing Units			Scope Reference
Bit 0 on	Selected Alert 1	B1C4 Receiver (Swap with B1B4)	B1R2 Gating	B1F2 ND Reg (Swap with B1L2)	RG403 Input to ND Register
Bit 1 on	Select Active	B1B2 Receiver (Swap with B1B4)	B1R2 Gating	B1F2 ND Reg (Swap with B1L2)	RG403 Input to ND Register
Bit 2 on	Sync In	B1B2 Receiver (Swap with B1B4)	B1R2 Gating	B1F2 ND Reg (Swap with B1L2)	RG403 Input to ND Register
Bit 3 on	Ignore	——	——	——	——
Bit 4 on	Normal End	B1C4 Receiver (Swap with B1B4)	B1R2 Gating	B1F2 ND Reg (Swap with B1L2)	RG403 Input to ND Register
Bit 5 on	Check End	B1C4 Receiver (Swap with B1B4)	B1R2 Gating	B1F2 ND Reg (Swap with B1L2)	RG403 Input to ND Register
Bit 6 on	Tag Valid	B1B2 Receiver (Swap with B1B4)	B1R2 Gating	B1F2 ND Reg (Swap with B1L2)	RG403 Input to ND Register
Bit 7	Unused	——	——	——	——

Hot Outbound Line (error code 8E46 when cable installed, error code 8E48 when disconnected)

Message Byte 2	Hot Inbound Line	Probable Failing Units		Scope Reference
Bit 0 on	Tag Gate	B1C4 Driver (Swap with B1B4)	B1M2 TB Register (Swap with B1L2)	GA502 Driver
Bit 1 on	Tag Bus 0	B1C2 Driver (Swap with B1B4)	B1F2 TD Register (Swap with B1L2)	GA602 Driver
Bit 2 on	Tag Bus 7	B1C2 Driver (Swap with B1B4)	B1F2 TD Register (Swap with B1L2)	GA602 Driver
Bit 3 on	Ignore	——	——	——
Bit 4 on	Tag Bus 5	B1C2 Driver (Swap with B1B4)	B1F2 TD Register (Swap with B1L2)	GA602 Driver
Bit 5 on	Tag Bus 6	B1C2 Driver (Swap with B1B4)	B1F2 Driver (Swap with B1L2)	GA602 Driver
Bit 6 on	Tag Bus 4 or	B1C2 Driver (Swap with B1B4)	B1F2 TD Register (Swap with B1L2)	GA602 Driver
	Recycle	B1C4 Driver (Swap with B1B4)	B1Q2 Recycle	GA502 Driver
Bit 7	Unused	——	——	——

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (Control Interface Wraparound)

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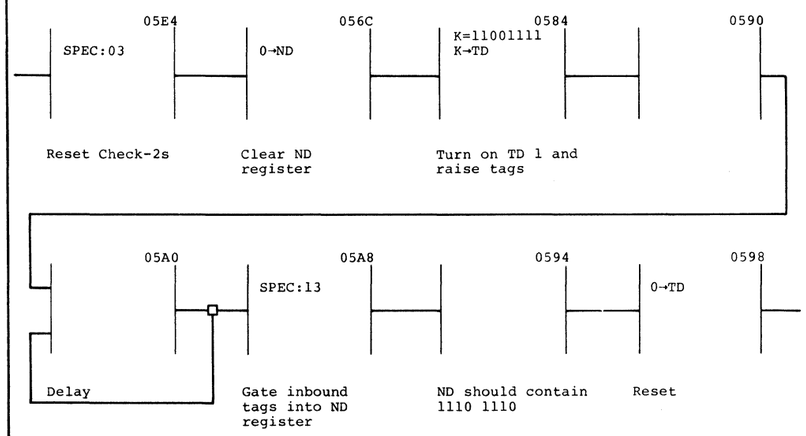
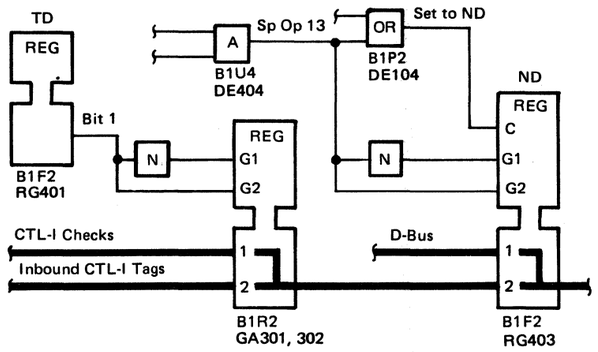
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8E48	B1R2 Gating B1F2 ND and TD Register (Swap with B1L2) B1U4 Special Op 13 B1P2 CD Decode	**CTL-I wraparound cable not installed—or—inbound CTL-I tags did not load into the ND register.** The ND register was set to zero and several inbound tags were raised. Then an attempt was made to gate the inbound tags into the ND register by performing a Special Op 13 with TD register bit 1=1. After Op 13, the ND register was examined and it still contained zero. Either the selector at B1R2 did not gate the tags to the ND register, or Op 13 did not set the tags into the ND register. *Note: The D-bus is 0010 0000 when the Special Op 13 is performed (caused by the delay microword 05A0).* If the ND register contains 0010 0000 after Special Op 13, the D-bus was gated into the ND register instead of the tags.	RG403 ND register	05E4-0598	



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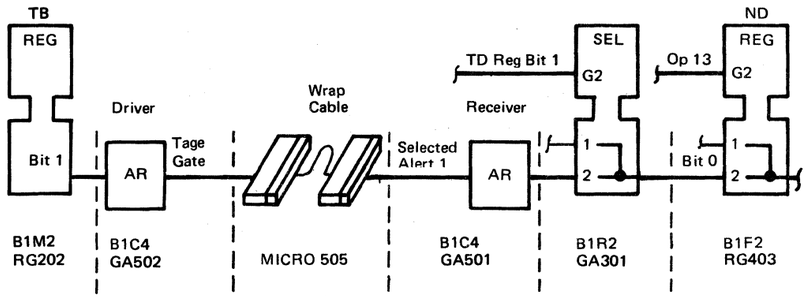
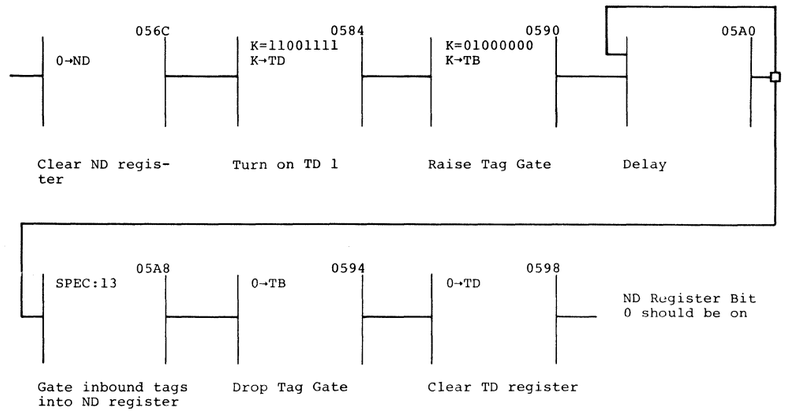
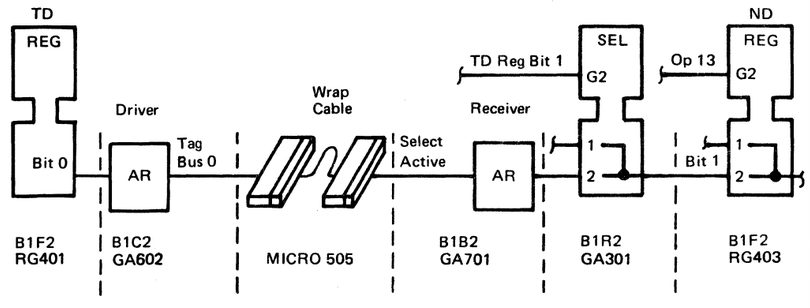
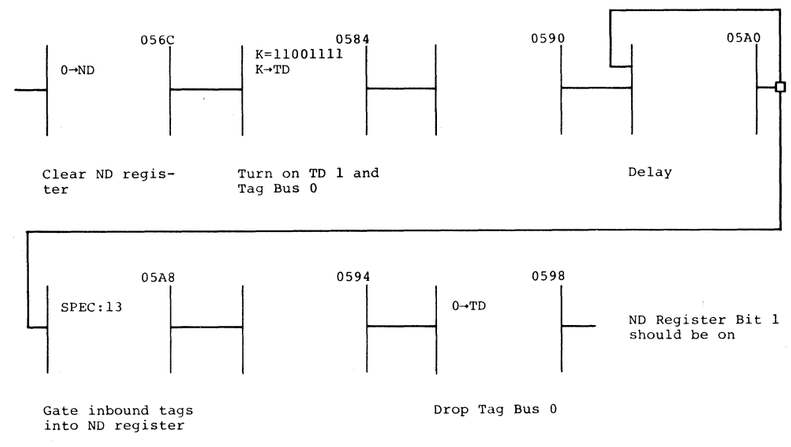
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8E50	B1R2 Gating B1C4 Driver/Receiver (Swap with B1B4) B1M2 TB Register (Swap with B1L2) B1F2 ND Register (Swap with B1L2)	**Tag Gate raised—Selected Alert 1 not received.** Outbound Tag Gate was raised. Tag Gate is turned around by the wrap cable to become inbound Selected Alert 1. Selected Alert 1 was checked by gating it into the ND register with a Special Op 13. 	RG403 ND register MICRO 505 Driver, receiver, and cables	056C-0598	
8E52	B1R2 Gating B1C2 Driver (Swap with B1B4) B1B2 Receiver (Swap with B1B4) B1F2 TD and ND Register (Swap with B1L2)	**Tag Bus 0 raised - Select Active not received.** Outbound Tag Bus 0 was raised. Tag Bus 0 is turned around by the wrap cable to become inbound Select Active. Select Active was checked by gating it into the ND register with a Special Op 13. 	RG403 ND register MICRO 505 Driver, receiver and cables	056C-0598	

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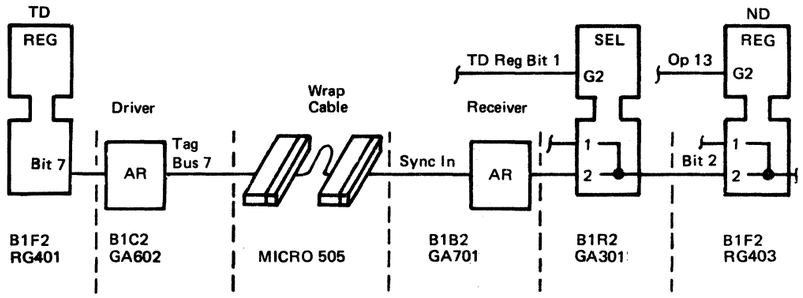
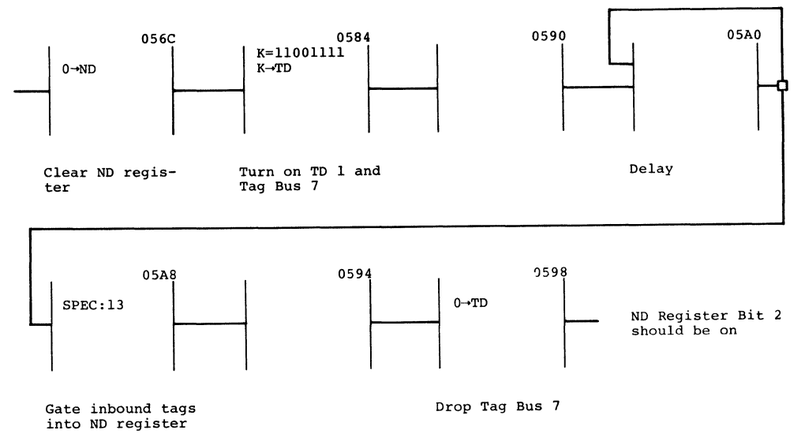
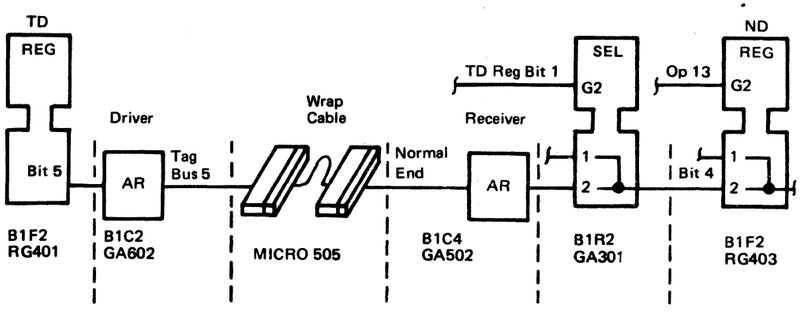
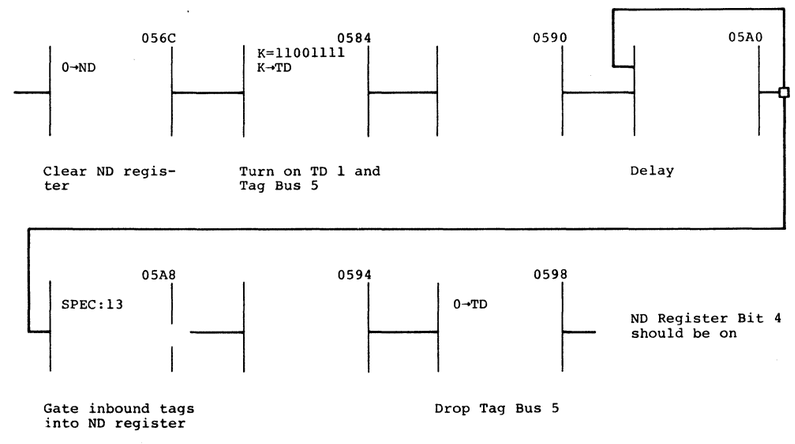
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8E54	B1R2 Gating B1C2 Driver (Swap with B1B4) B1B2 Receiver (Swap with B1B4) B1F2 TD and ND Register (Swap with B1L2)	**Wraparound cable in backward or Tag Bus 7 raised—Sync In not received.** Outbound Tag Bus 7 was raised. Tag Bus 7 is turned around by the wrap cable to become Sync In. Sync In was checked by gating it into the ND register with a Special Op 13. 	RG403 ND register MICRO 505 Driver, receiver and cables	056C-0598	
8E56	B1R2 Gating B1C2 Driver (Swap with B1B4) B1C4 Receiver (Swap with B1B4) B1F2 ND and TD Register (Swap with B1L2)	**Tag Bus 5 raised—Normal End not received.** Outbound Tag Bus 5 was raised. Tag Bus 5 is turned around by the wrap cable to become inbound Normal End. Normal End was checked by gating it into the ND register with a Special Op 13. 	RG403 ND register MICRO 505 Driver, receiver, and cables	056C-0598	

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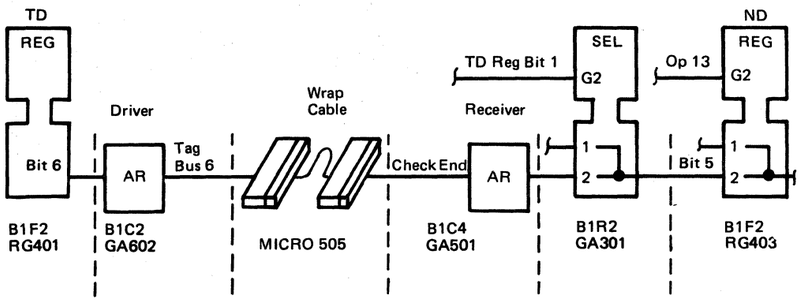
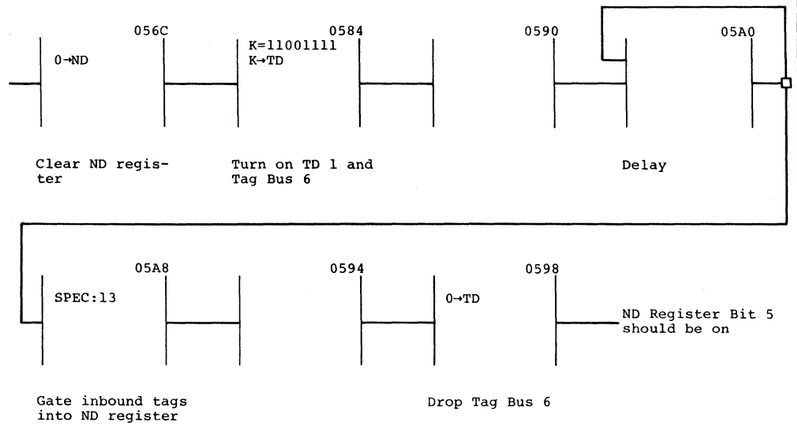
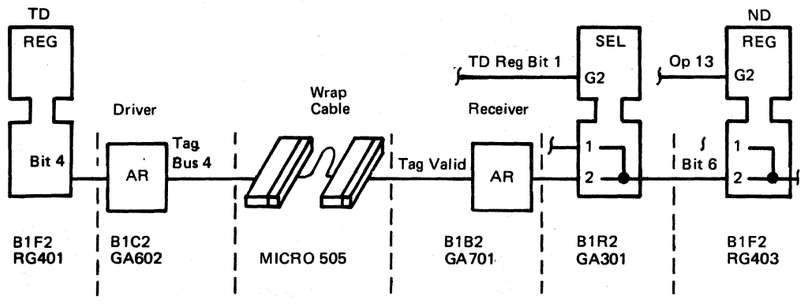
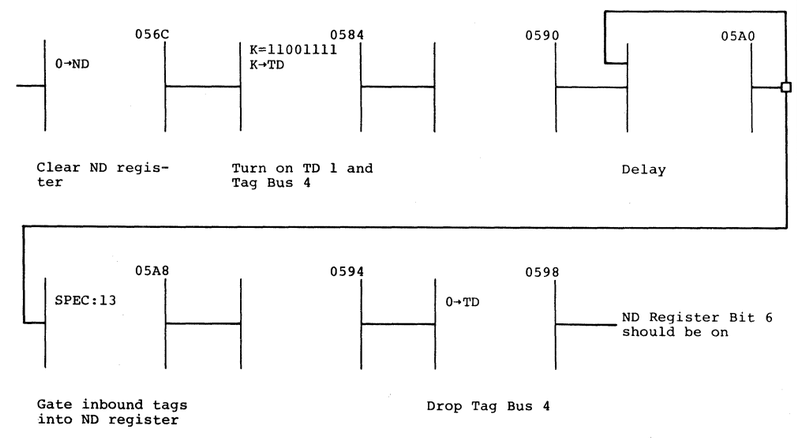
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
8E58	B1R2 Gating B1C2 Driver (Swap with B1B4) B1C4 Receiver (Swap with B1B4) B1F2 TD and ND Register (Swap with B1L2)	**Tag Bus 6 raised—Check End not received.** Outbound Tag Bus 6 was raised. Tag Bus 6 is turned around by the wrap cable to become inbound Check End. Check End was checked by gating it into the ND register with a Special Op 13. 	RG403 ND register MICRO 505 Driver, receiver, and cables	056C-0598	
8E5A	B1R2 Gating B1C2 Driver (Swap with B1B4) B1B2 Receiver (Swap with B1B4) B1F2 TDand ND Register (Swap with B1L2)	**Tag Bus 4 raised—Tag Valid not received.** Outbound Tag Bus 4 was raised. Tag Bus 4 is turned around by the wrap cable to become inbound Tag Valid. Tag Valid was checked by gating it into the ND register with a Special Op 13. 	RG403 ND register MICRO 505 Driver, receiver, and cables	056C-0598	

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MICRODIAGNOSTIC ERROR CODE DICTIONARY (Control Interface Wraparound)

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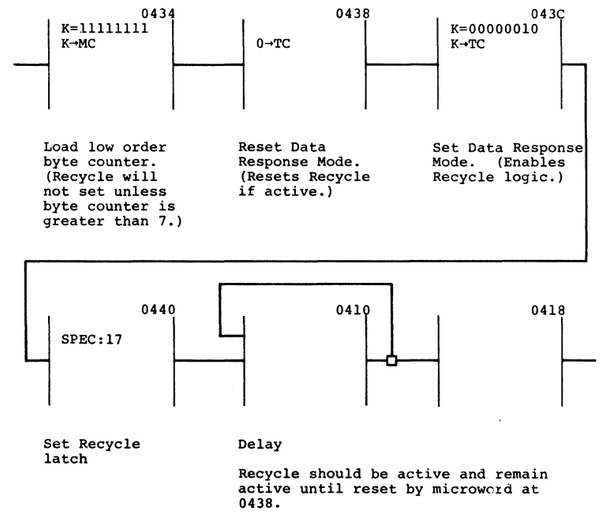
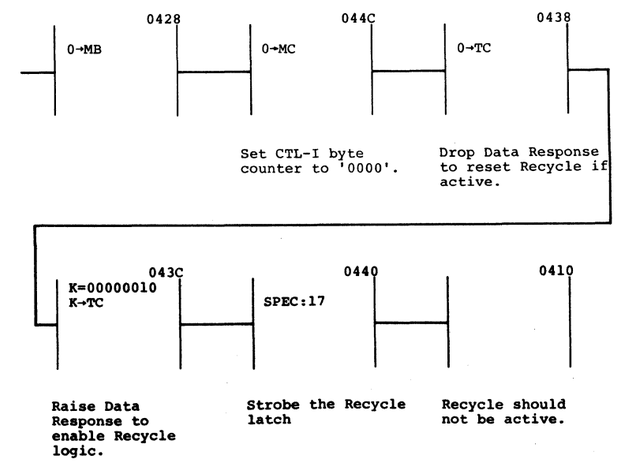
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
9060	B1Q2 Recycle Logic B1C4 Recycle Driver (Swap with B1B4) B1U4 Special Op 17	**Recycle failure.** This routine tests the ability to set the Recycle latch and the Recycle driver and cable. The CAS shown was executed and should have set the Recycle latch. Recycle is returned by the wrap cable as Tag Valid. When examined, Tag Valid was inactive. This indicates that either Recycle did not set, Recycle reset prematurely, or the Recycle driver or cable is defective.	GA201 Recycle logic MICRO 505 Driver and cables	0434-0418	
9062	B1Q2 Recycle Logic B1M2 High Order Byte Counter (Swap with B1E2) B1L2 Low Order Byte Counter (Swap with B1E2)	**Recycle failure.** This routine checks the Recycle latch to ensure that it will not set when the control interface byte counter contains a value less than 8. The CAS shown was executed, and Recycle should not have set. Recycle is returned by the wrap cable as Tag Valid. When examined, Tag Valid was active. This indicates that either the Recycle logic is defective, or the byte counter (MB and MC registers) is passing a hot bit to the Recycle logic.	GA201 Recycle logic RG202 MB register RG302 MC register	0428-0410	

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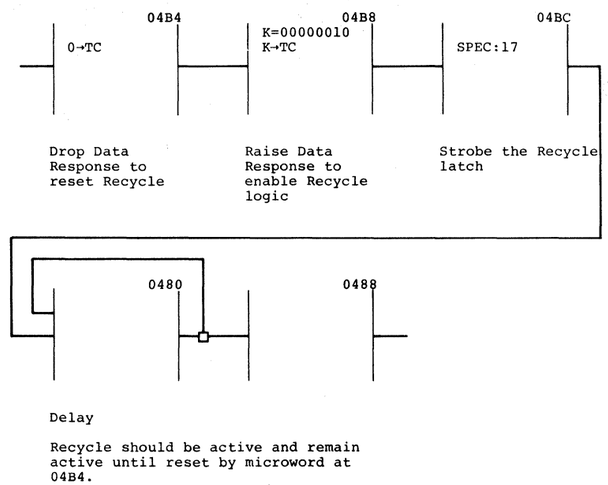
9064	B1Q2 Recycle Logic B1M2 High Order Byte Counter (Swap with B1E2) B1L2 Low Order Byte Counter (Swap with B1E2)	**Recycle failure.** This routine checks each bit position of the control interface byte counter (MB and MC registers) to ensure that the Recycle latch can be set when they are active. The second and third error message bytes indicate which bit failed. Byte 2 contains the contents of the MB register (high order byte of the byte counter), and byte 3 contains the contents of the MC register (low order byte of the byte counter) at the time of failure. To scope, manually load the MB and MC registers with the values in the second and third message bytes, respectively; then recycle the CAS shown.	GA201 Recycle logic RG202 MB register RG302 MC register	04B4-0488	

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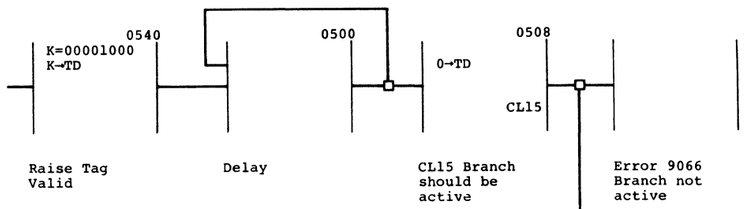
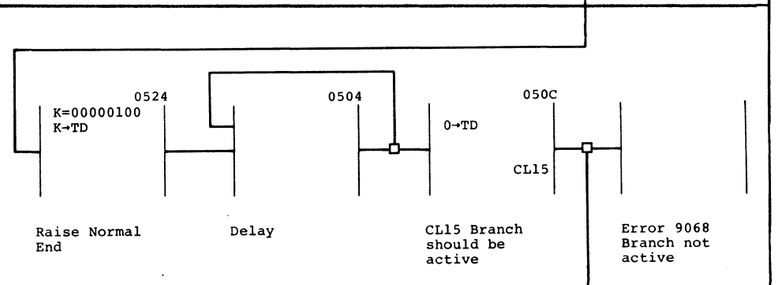
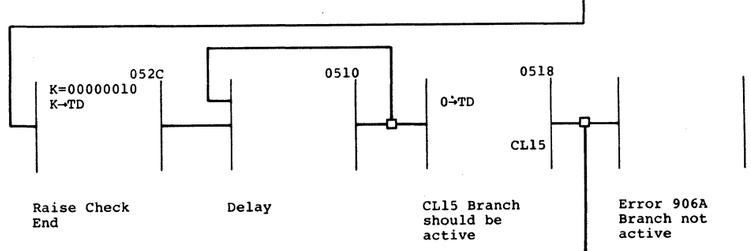
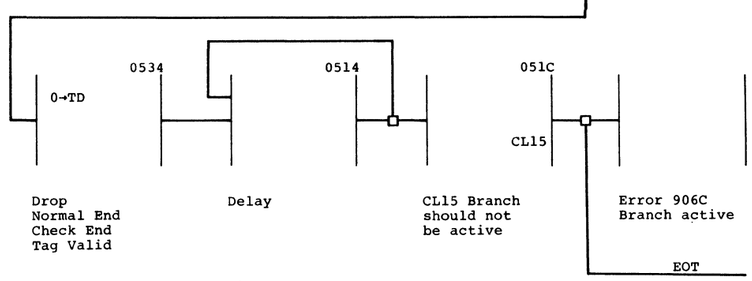
9066	B1R2 CL15 Logic B2L2 CL15 Branch AIR2 Alternate CL15	**CL15 branch failure.** Tag Bus Bit 4, which is returned by the wrap cable as Tag Valid, was raised. Tag Valid should have caused a CL15 branch.	GA301 CL15	0540-0508	
9068	B1R2 CL15 Logic B1D2 Feed-Through	**CL15 branch failure.** Tag Bus Bit 5, which is returned by the wrap cable as Normal End, was raised. Normal End should have caused a CL15 branch.	GA301 CL15 GA104 N.E. feed thru	0524-050C	
906A	B1R2 CL15 Logic B1D2 Feed-Through	**CL15 branch failure.** Tag Bus Bit 6, which is returned by the wrap cable as Check End, was raised. Check End should have caused a CL15 branch.	GA301 CL15 GA104 C.E. feed thru	052C-0518	
906C	B1R2 CL15 Logic B2L2 CL15 Branch AIR2 Alternate CL15	**Hot CL15 branch.** The three tags (Normal End, Check End, and Tag Valid) that cause a CL15 branch were made inactive. When tested, CL15 was active. If the suggested recycle loop will not duplicate the error, try recycling from the beginning of the test 0540-051C.	GA301 CL15	0534-051C	

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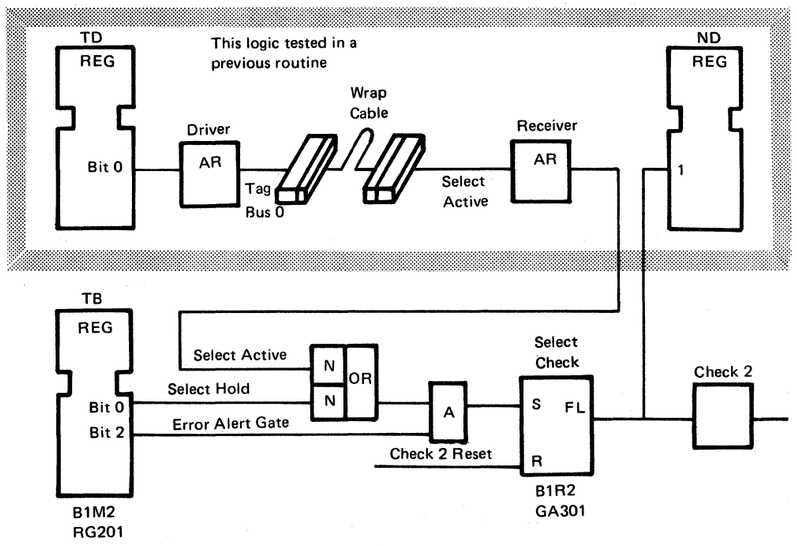
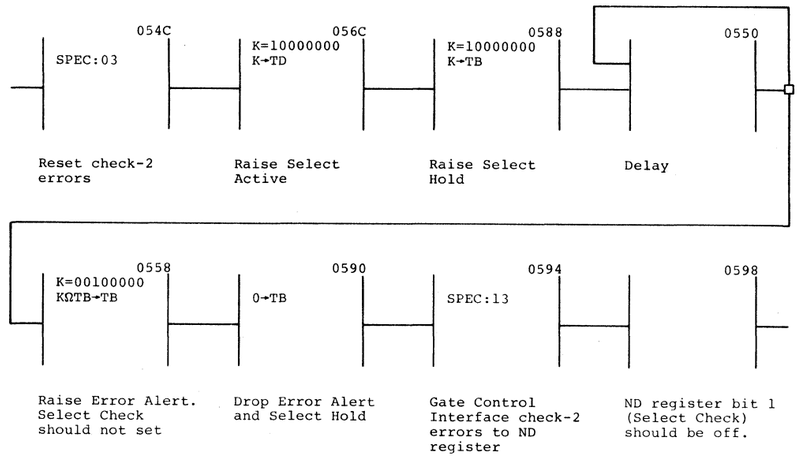
9070	B1R2 Select Check Logic B1M2 TB Register (Swap with B1E2) B1F2 TD Register (Swap with B1E2)	**False Select Check.** The Select Check circuit was tested by raising Select Active and Select Hold, then strobing the Select Check latch with Error Alert. The latch should not have set, but when tested, ND register bit 1 (Select Check) was on.	GA301 Select Check Logic	054C-0598	





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9072	B1R2 Select Check Logic B1M2 TB Register (Swap with B1E2)	**Select Check failed to set.** The Select Check circuit was tested by raising Select Hold, dropping Select Active, then strobing the Select Check latch with Error Alert. (See error code 9070 for block diagram.) The Select Check latch should have set, but when tested, ND register bit 1 (Select Check) was off.	GA301 Select Check Logic	0584-05B8	0584 SPEC:03 — Reset check-2 errors 05D0 0→TD — Turn off Select Active 05A4 K=10000000 K→TB — Raise Select Hold 05A8 K=00100000 KΩTB→TB — Raise Error Alert. Select Check should set 05AC 0→TB — Drop Error Alert and Select Hold 05B0 SPEC:13 — Gate Control Interface check-2 errors to ND register 05B4 — ND register Bit 1 (Select Check) should be on 05B8 0→ND — Clear ND register
9074	B1R2 Select Check Logic B1M2 TB Register (Swap with B1E2)	**Select Check failed to set.** The Select Check circuit was tested by raising Select Active, dropping Select Hold, then strobing the Select Check latch with Error Alert. (See error code 9070 for block diagram.) The Select Check latch should have set, but when tested, ND register bit 1 (Select Check) was off.	GA301 Select Check Logic	0578-05C8	0578 SPEC:03 — Reset check-2 errors 05BC K=10000000 K→TD — Raise Select Active 05D4 0→ND — Clear check-2 register 0554 — Delay 055C K=00100000 K→TB — Raise Error Alert. Select Check should set 05C0 0→TB — Drop Error Alert 05C4 SPEC:13 — Gate Control Interface check-2 errors to ND register 05C8 — ND register bit 1 (Select Check) should be on.

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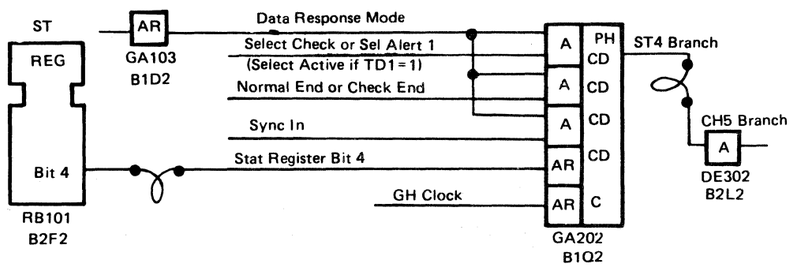
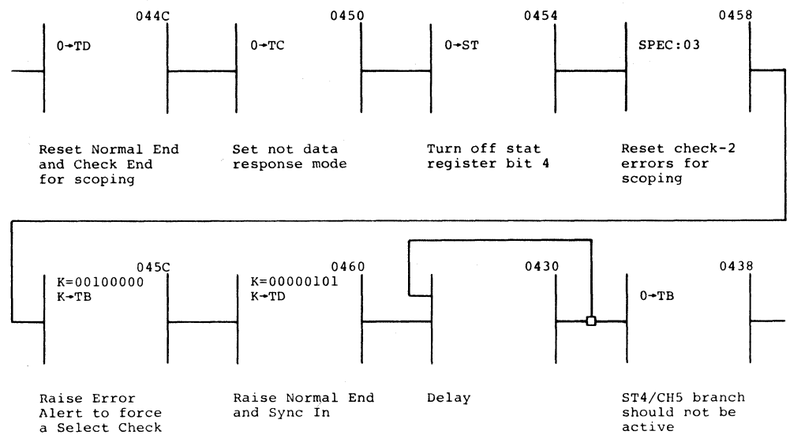
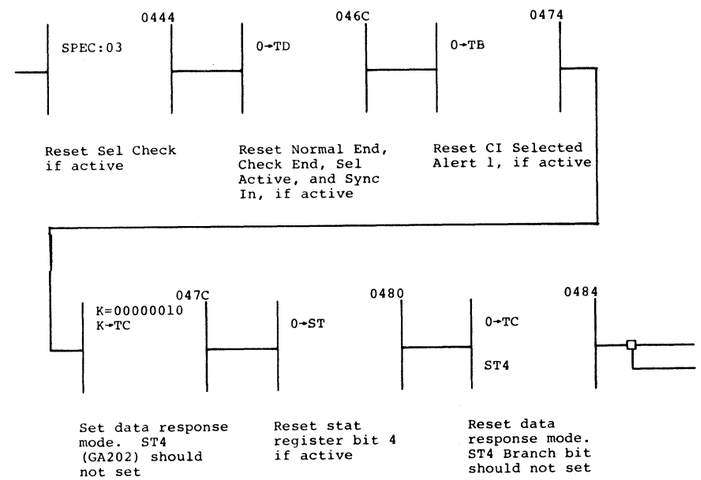
9278	B1Q2 ST4 Gating B1D2 Data Response Trileads from B2 to B1 board and B1 to B2 board B2L2 ST Register B2F2 Branch Bit	**ST4 Branch set when logic is not in data response mode.** Sync In, Normal End, and Select Check were raised. Any one of these should cause an ST4 branch if the CTL-I logic is in the data response mode. During this routine, the logic was NOT in data response mode (TC register = '00'), and ST4 should have been degated. When tested, ST4 was active. 	GA202 ST4 Gating GA103 Data Response	044C-0438	
927C	B1Q2 ST4 Gating B1D2 Sync In Latch B2N2 Clock	**ST4 Branch active with no inputs active.** All inputs to the ST4 branch logic that should cause a branch were reset. The control interface logic was then placed in the data response mode and a test branch was made. ST4 (CH5) Branch was active. See error code 9278 for block diagram of ST4.	GA202 ST4 Gating	0444-0484	

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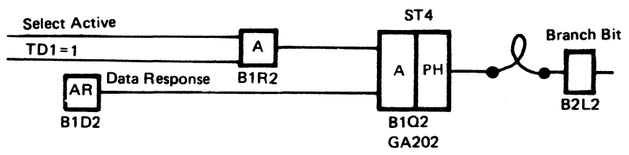
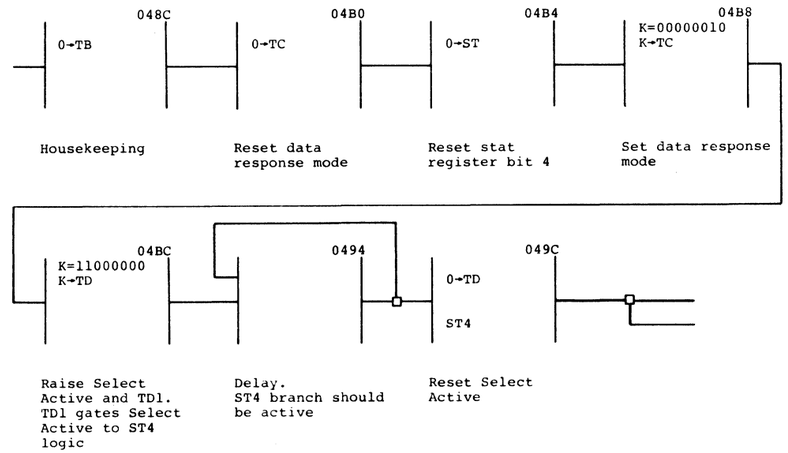
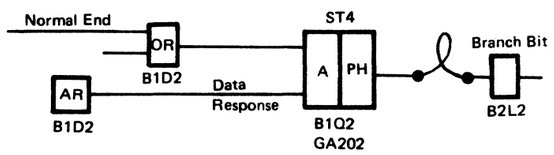
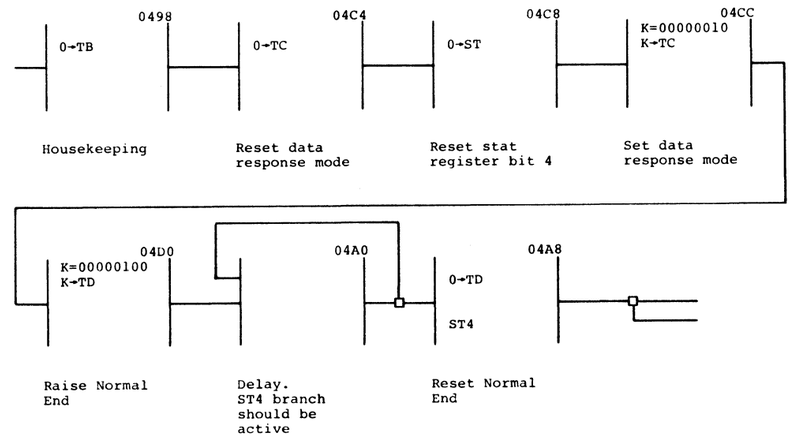
9280	B1Q2 ST4 Branch Logic B1R2 Select Active Gating B1D2 Data Response B2F2 Branch Bit	**Select Active did not cause ST4 branch.** Tag Bus 0, which is returned by the wrap cable as Select Active, was raised. Select Active should have been gated to the ST4 logic (TD register bit 1 was on), and should have caused a branch (logic was in data response mode). 	GA202 ST4 Branch Logic GA301 Select Active Gating	048C-049C	
9282	B1Q2 ST4 Branch Logic	**Normal End did not cause ST4 branch.** Tag Bus 5, which is returned by the wrap cable as Normal End, was raised. The CTL-I logic was in the data response mode, so Normal End should have caused an ST4 branch. 	GA202 ST4 Branch Logic	0498-04A8	

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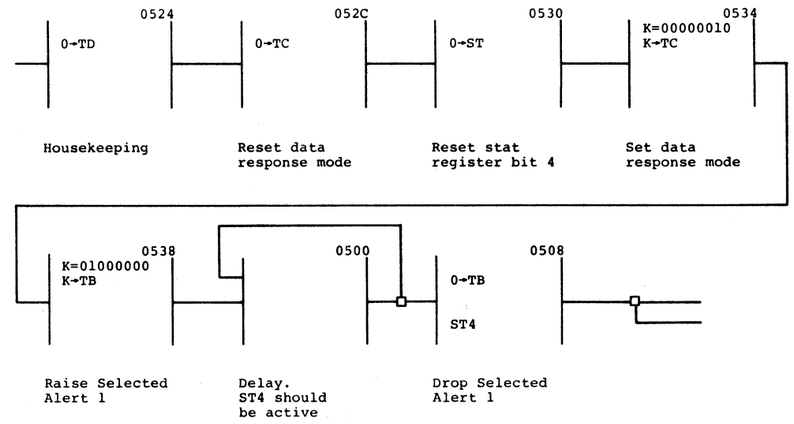
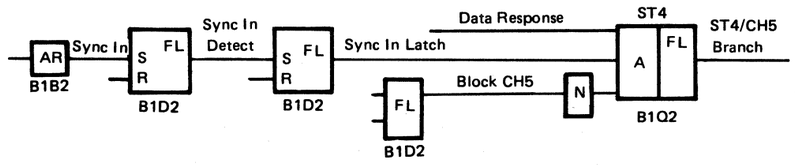
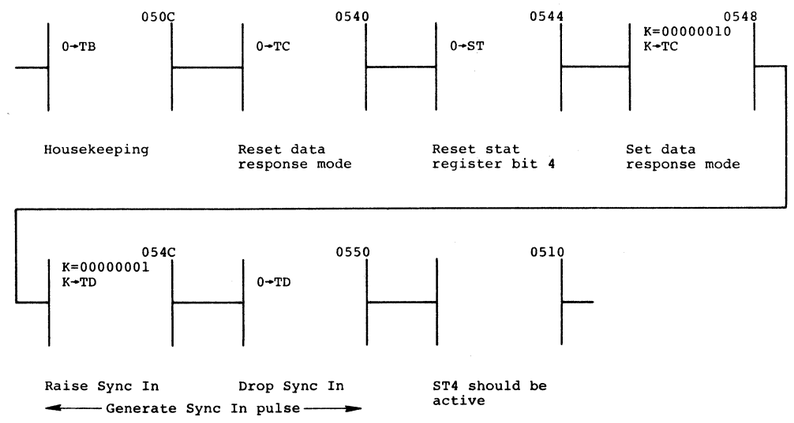
9284	B1Q2 ST4 Logic	**Selected Alert 1 did not cause ST4 branch.** TB register bit 1 (Tag Gate), which is returned by the wrap cable as Selected Alert 1, was raised. Selected Alert 1 should have caused an ST4 branch.	GA202 ST4 Logic	0524-0508	
9286	B1D2 Sync In Logic B1Q2 ST4 Logic B2N2 Clock	**Sync In did not cause ST4 branch.** A Sync In pulse was generated with the CTL-I logic in the data response mode. ST4 should have set. 	GA202 ST4 Logic GA103 Sync In Latches	050C-0510	

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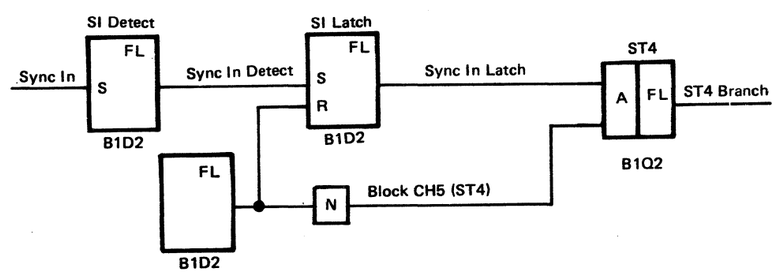
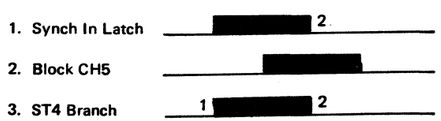
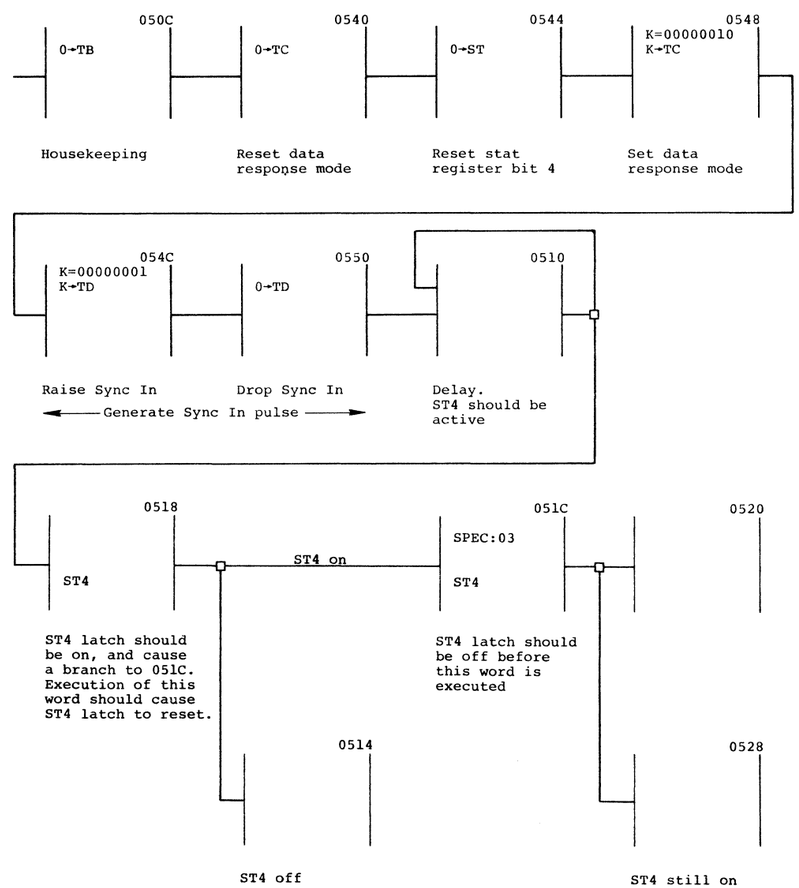
9288	B1D2 Sync In Logic B1Q2 ST4 Logic	**Two ST4 branches for one Sync In pulse.** One and only one ST4 branch should occur for each Sync In pulse. When the microprogram branches on ST4 it is sensed by the logic, then ST4 latch is reset. The test routine generates a Sync In pulse, then executes two successive microwords containing ST4 branches. ST4 latch should be on for the first branch, reset for the second. When the second branch was executed, ST4 latch was still on. *Note: If the CAS logic shown is single-cycled, check-2 errors may occur and ST4 latch may be off when the first branch is executed. These conditions are normal and should be ignored.*   	GA202 ST4 Logic GA103 Sync In Logic	050C-051C	

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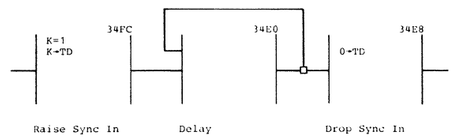
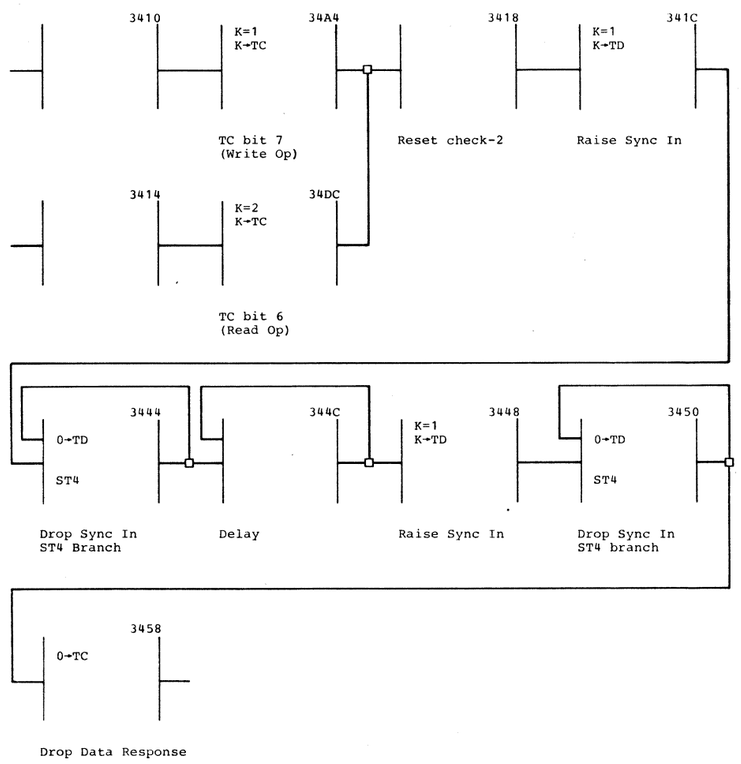
92A0	B1D2 CTL-I Buffer and Control Card	A CTL-I Transfer Check was detected while not in a data response mode. This indicates that either the Data Response line is on solidly or that a solid Transfer Check exists.	GA103 —Data Response GA104 CTL-I Transfer Error	34FC-34E8	
92A1 **92A2**	B1D2 CTL-I Buffer and Control Card	This routine simulates a Write sequence and then a Read sequence to verify the normal operation of the CTL-I Transfer Check circuitry. **92A1** Transfer Check error during a Write operation. **92A2** Transfer Check error during a Read operation.	GA103 Data Response, Sync In Detected, CH Branch Bit GA104 CTL-I Transfer Error	 3410-3458 3414-3458	

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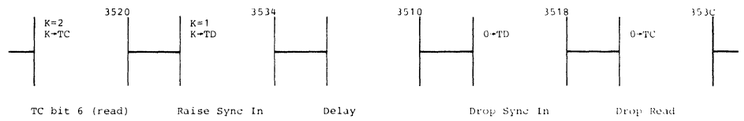
92A3 92A4 92A5	B1D2 B1R2 CTL-I Checks	This routine is designed to exercise the CTL-I Transfer Check circuitry by simulating a solid Sync In pulse. A Transfer Check should occur if Sync In is held on for more than 300 ns. The three error codes indicate different stages of failure as follows: **92A3** A check-2 error was not detected. **92A4** A check-2 error was detected, but it was not a CTL-I check-2. Second error message byte = NA register. Third error message byte = ND register. **92A5** A CTL-I check-2 error was detected, but it was not a CTL-I Transfer Check. Second error message byte = ND register.	GA103 +Sync In Detected GA104 CTL-I Transfer Error GA301 ND Register	3520-353C	

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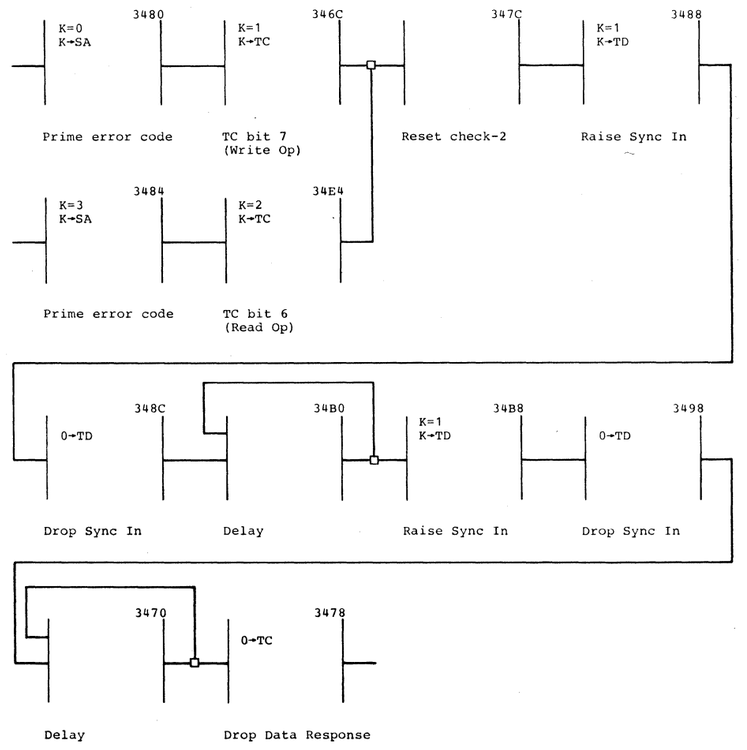
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
92A6 92A7 92A8 92A9 92AA 92AB	B1D2 CTL-I Buffer and Control Card	This routine is designed to exercise the CTL-I Transfer Check circuitry by simulating an ST4 branch failure. A Transfer Check should occur in either a Write or Read operation if an ST4 branch is not taken between two successive Sync In pulses. The error codes indicate that a Transfer Check did not occur as expected in either a write (92A6-92A8) or read (92A9-92AB) mode of operation. **Write / Read / Error Description** 92A6 or 92A9 — No check-2 error — expected CTL-I check-2 error (NA register bit 4) 92A7 or 92AA — A CTL-I check-2 error was detected, but it was not a CTL-I Transfer Check (ND register bit 6). Second error message byte contains the ND register. 92A8 or 92AB — A check-2 was detected, but it was not a CTL-I check-2. Second error message byte contains the NA register. Third error message byte contains the ND register.	GA103 Data Response, Sync In Detected, CH Branch Bit GA104 CTL-I Transfer Error	(Write) 3480-3478 (Read) 3484-3478	

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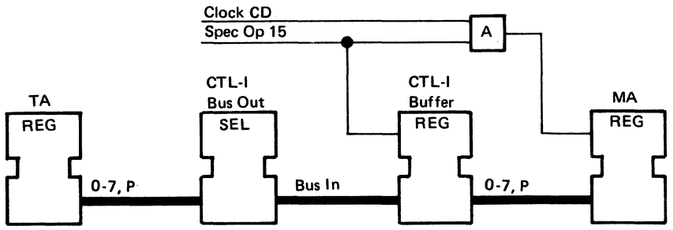
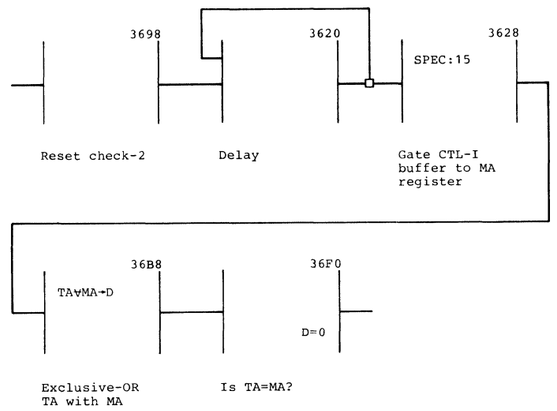
Error Code	Probable Failing Replaceable Units	Error Description and Comments (Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)	Scope Reference	Recycle Addresses (IAR-ACR)	CAS (Refer to PANEL 16 for recycle procedure).
92B0 92B1 92B2	B1D2 CTL-I Buffer and Control Card B1E2 TA and MA Register B1B4 Driver B1B2 Driver/Receiver B1C2 Receiver Cables B1U4 Spec Op 15 B1R2 CTL-I Checks	 This routine checks the data path shown above. The TA register is loaded into the CTL-I bus out when not in a Data Response mode of operation. The bus out is wrapped around as bus in. Spec Op 15 gates bus in to the CTL-I buffer, and gates the buffer to the MA register. At this point, the contents of the TA register should equal those of the MA register. If an error occurs during this operaiton, one of three error codes indicate the failure: **92B0** TA was equal to MA, but a CTL-I check-2 was detected. Either a Bus Out parity error or CTL-I Buffer Parity Error was detected. **92B1** TA was not equal to MA, and a check-2 was detected. **92B2** TA was not equal to MA, but no check-2 was detected. For all three error codes: Second error message byte contains the ND register. Third error message byte contains the TA register. Fourth error message byte contains the MA register.	GA101 CTL-I Buffer Bits, Buffer Parity Error, TA Reg Bits GA102 CTL-I Bus Out Bits, CTL-I Bus Out Parity Check GA103 Set Buffer, Spec Op 15 GA104 Gate External MA Reg RG101 RG102 TA and MA Reg Bits MICRO 505 Drivers, Receivers, Cables GA301 ND Reg Bits	3698-36F0	 *Note: When using the recycle loop, check that the value in the TA register is the same as displayed in error message byte 3. If it is not, be sure to load that value into the TA register.*

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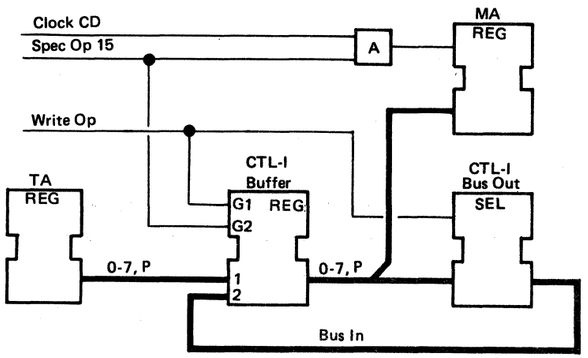
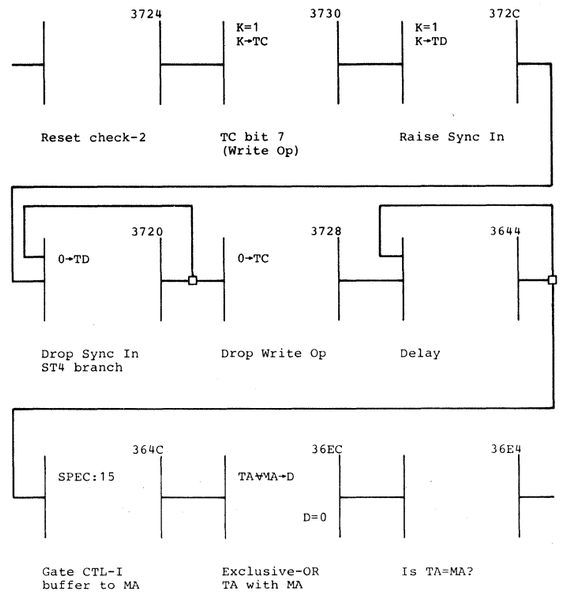
Error Code	Probable Failing Replaceable Units	Error Description and Comments (Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)	Scope Reference	Recycle Addresses (IAR-ACR)	CAS (Refer to PANEL 16 for recycle procedure).
92B3 **92B4** **92B5**	B1D2 CTL-I Buffer and Control Card B1E2 TA and MA Registers B1B4 Driver B1B2 Driver/Receiver B1C2 Receiver Cables	 This routine exercises the data paths illustrated above. During a Write operation, the TA register is gated to the CTL-I buffer. From the buffer, the data is gated to the CTL-I bus out, which is wrapped around as bus in. Then, Data Response is dropped and Spec Op 15 gates the bus in to the CTL-I buffer, and the buffer to the MA register. At this point, the contents of the TA register are exclusive-ORed with those of the MA register. They should be equal. If an error is detected during the cycle, one of three error codes is posted: **92B3** TA was equal to MA, but a CTL-I check-2 error was detected. The error may be Bus Out Parity check and/or buffer Parity check and/or Transfer Check (check byte 2). **92B4** TA was not equal to MA, and a check-2 error was detected. **92B5** TA was not equal to MA, but no check-2 error was detected. For all three error codes: Second error message byte contains the ND register. Third error message byte contains the TA register. Fourth error message byte contains the MA register.	GA101 CTL-I Buffer Bits, Buffer Parity Error, TA Register Bits GA102 CTL-I Bus Out Bits, CTL-I Bus Out Parity Check GA103 Set Buffer, Sync In Detected, Data Response GA104 CTL-I Transfer Error, Spec Op 15, Gate External MA Register RG101-102 TA and MA Register Bits MICRO 505 Drivers Receivers Cables	3724-36E4	 *Note: When using the recycle loop, make sure that the value in the TA register is the same as that displayed in error message byte 3.*

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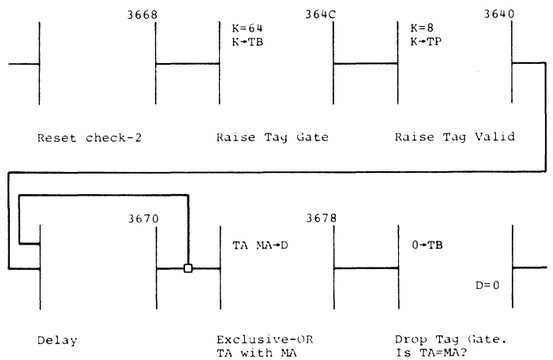
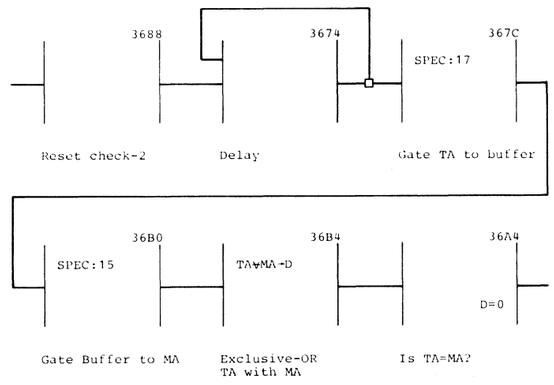
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
92B6	B1D2 CTL-I Buffer and Control Card B1E2 TA and MA Register B1Q2	This routine checks the gating of the CTL-I buffer to the MA register when not in a data response mode. This check is accomplished by raising Tag Gate and Tag Valid. This error code is posted if TA is not equal to MA after the following three steps have been executed: (1) bus in is loaded with the TA register contents, (2) Tag Gate and Tag Valid are used to gate bus in to the CTL-I buffer, and (3) the buffer contents are gated to the NA register. Second error message byte contains TA register. Third error message byte contains MA register.	GA101 CTL-I Buffer Bits GA103 Set Buffer GA104 CTL-I Tag Valid Synced, Tag Gate, Gate External MA Register RG101-102 TA and MA Register Bits MICRO 505 Drivers Receivers Cables	3668-36E8	 *Note: When using the recycle loop, make sure that the value in the TA register is the same as displayed in the second error message byte.*
92B7	B1D2 CTL-I Buffer and Control Card B1E2 TA and MA Registers B1U4 Spec Op 17 Spec Op 15	This routine verifies the gating of the TA register to the CTL-I buffer. To verify the gating: (1) a Special Op 17 loads the buffer, (2) a Special Op 15 gates the buffer contents to the MA register, and (3) TA is compared with MA. This error code results if TA is not equal to MA. Second error message byte contains the TA register. Third error message byte contains the MA register.	MICRO 505 Drivers Receivers Cables GA101 CTL-I Buffer Bits GA103 Set Buffer Spec Op 17 GA104 Spec Op 15, Gate External MA Register RG101-102 TA and MA Register Bits	3688-36A4	 *Note: When using the recycle loop, make sure that the value in the TA register is the same as displayed in error message byte 2.*

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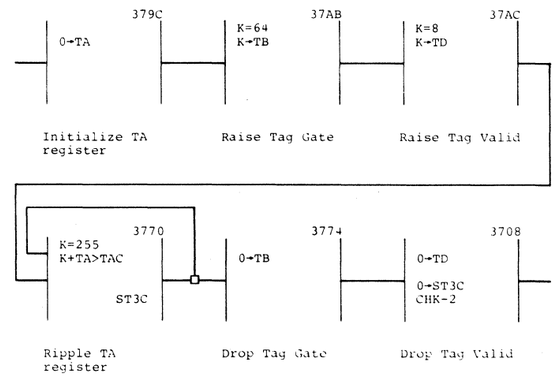
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
92B8 **92B9** **92BA**	B1D2 CTL-I Buffer and Control Card B1R2 CTL-I Checks	This routine exercises the CTL-I bus out and CTL-I buffer parity checkers. The exercise consists of changing the bus while Tag Gate is active. This change causes both a Bus Out Parity Error and a CTL-I Buffer Parity Error. **92B8** No check-2 detected. A CTL-I check-2 was expected. **92B9** A check-2 was detected, but not a CTL-I check-2. **92BA** A CTL-I check-2 was detected, but neither Bus Out Parity error nor Buffer Parity error was detected. For all three error codes: Second error message byte contains the NA register. Third error message byte contains the ND register.	GA101 Buffer Parity Error GA102 Bus Out Parity Error GA103 Set Buffer GA104 Tag Gate CTL-I Tag Valid Synced, Gate External MA Register MICRO 505 Drivers Receivers Cables GA301 ND Register Bits	379C-3708	

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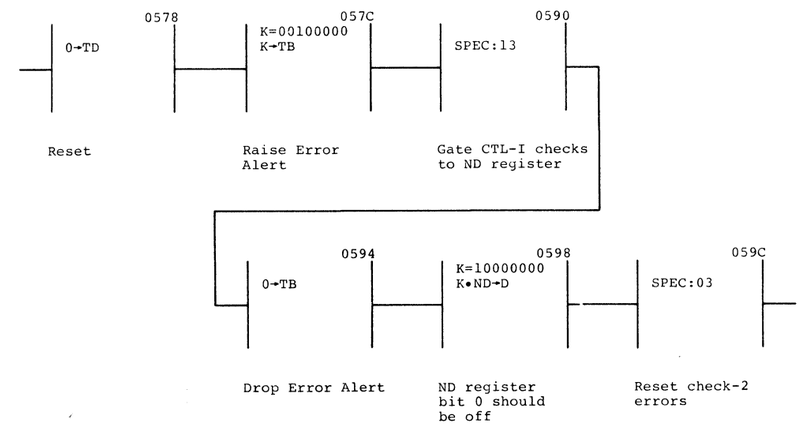
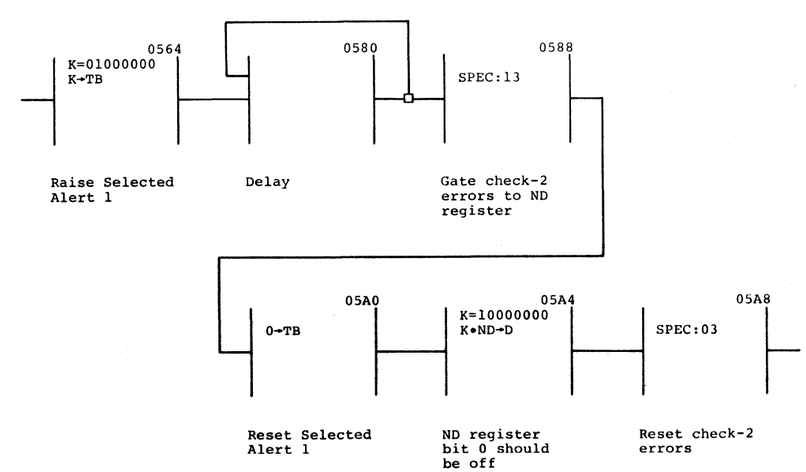
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
92D0	B1R2 Controller Check	**Controller Check set without Selected Alert 1.** The controller check latch was tested by raising Error Alert without Selected Alert 1 (controller check). The controller check latch should not have set, but when CTL-I check-2 errors were gated to the ND register, bit 0 (controller check) was on. When recycling, Select Active Check will set and cause ND register bit 1 to turn on. This is normal and should be ignored.	GA301 Controller Check	0578-059C	
92D2	B1R2 Controller Check	**Controller Check set without Error Alert.** The controller check latch was tested by raising Selected Alert 1 (controller check) without Error Alert. The controller check latch should not have set, but when CTL-I check-2 errors were gated to the ND register, bit 0 (controller check) was on.	GA301 Controller Check	0564-05A8	

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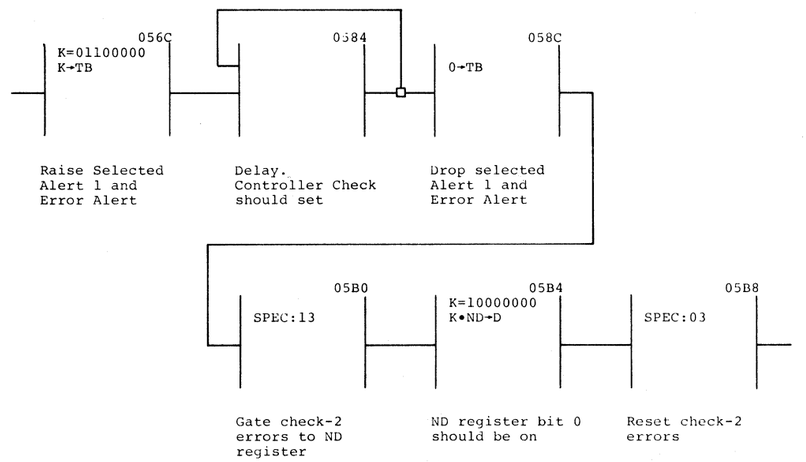
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
92D4	B1R2 Controller Check	**Controller Check not set.** Selected Alert 1 (controller check) and Error Alert were raised. Controller check should have set, but when CTL-I check-2 errors were gated to the ND register, bit 0 (controller check) was not active. When recycling, Select Active Check will set and cause ND register bit 1 to turn on. This is normal and should be ignored.	GA301 Controller Check	056C-05B8	

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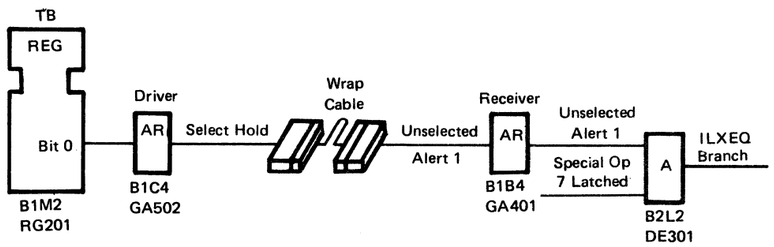
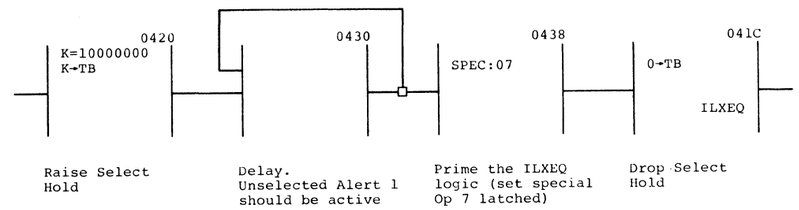
Error Code	Probable Failing Replaceable Units	Error Description and Comments	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
94D6	B1C4 Select Hold Driver (Swap with B1C2) B1B4 Unselected Alert 1 Receiver (Swap with B1B2) B1M2 TB Register (Swap with B1E2) B2L2 ILXEQ Branch	**Select Hold raised — Unselected Alert 1 not received.** TB register bit 0, which is the CTL-I outbound tag Select Hold, was raised. Select Hold is returned by the wrap cable as Unselected Alert 1, which should cause an ILXEQ branch when active. When tested, ILXEQ was inactive. 	GA502 Select Hold GA401 Unselected Alert 1 DE301 ILXEQ	0420-041C	

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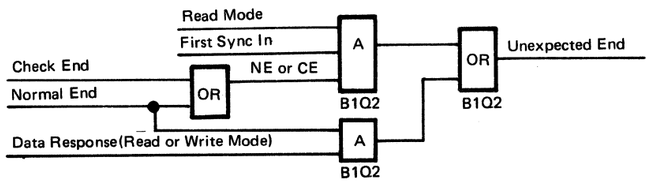
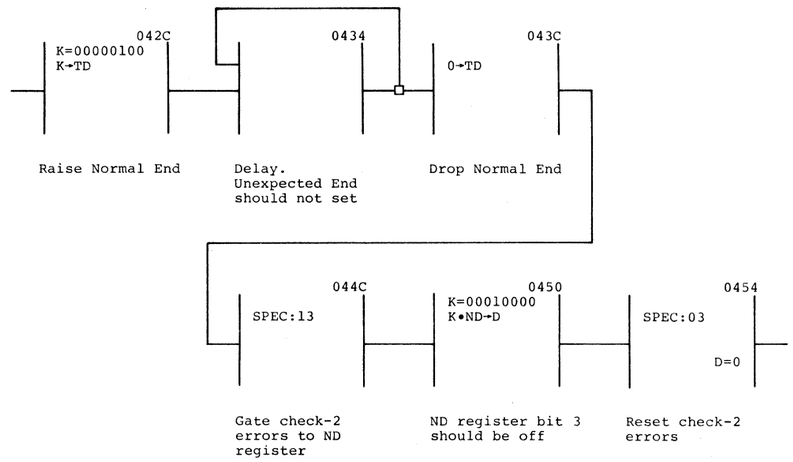
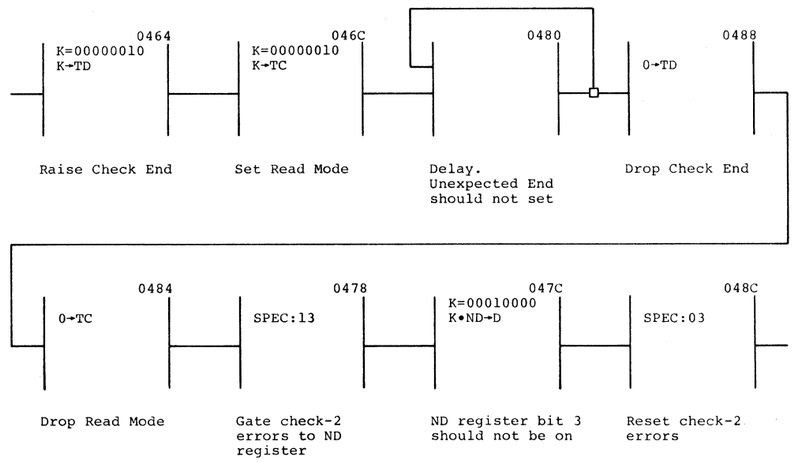
Error Code	Probable Failing Replaceable Units	Error Description and Comments	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
94D8	B1Q2 Unexpected End Logic B1F2 ND Register (Swap with B1E2)	**Unexpected End set without logic in data response mode.** Unexpected End should set if Normal End is received when the CTL-I logic is in data response mode. During this test, Normal End was active but the logic was not in data response mode, and Unexpected End should not have set. When examined, ND register bit 3 (Unexpected End Check) was active. 	GA201 Unexpected End	042C-0454	
94DA	B1Q2 Unexpected End Logic B1D2 1st Sync In Logic	**Unexpected End set without 1st Sync In or Normal End.** The CTL-I logic was placed in read mode, and Check End was raised. Unexpected End should not have set, but when examined, ND register bit 3 (Unexpected End Check) was active. See error code 94D8 for block diagram of Unexpected End logic.	GA201 Unexpected End	0464-048C	

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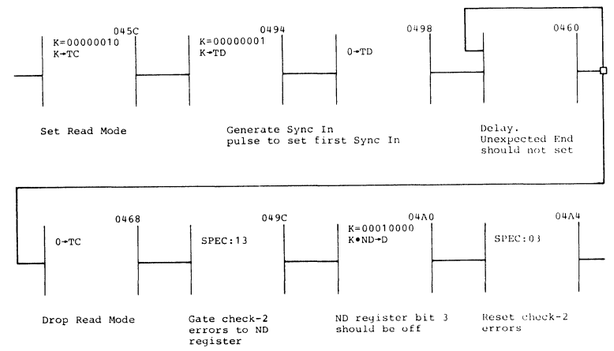
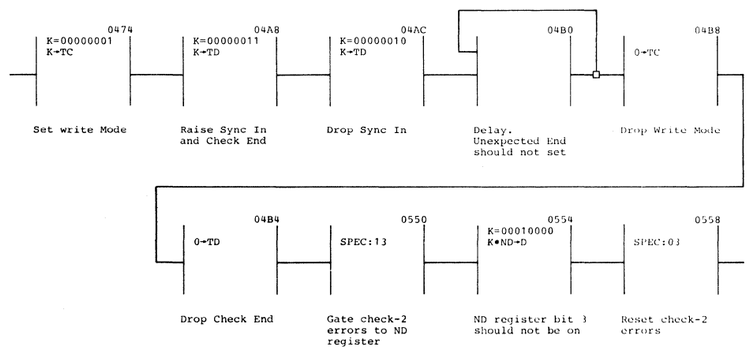
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
94DC	B1Q2 Unexpected End Logic	**Unexpected End set without Normal End or Check End active.** The CTL-I logic was placed in read mode, and a Sync In pulse was generated. Neither Normal End nor Check End was active, so Unexpected End should not have set. When examined, ND register bit 3 (Unexpected End Check) was active. See error code 94D8 for block diagram of Unexpected End logic. If the CAS logic shown is single-cycled, check-2 errors (transfer checks) may occur and should be ignored.	GA201 Unexpected End	045C-04A4	
94DE	B1Q2 Unexpected End Logic	**Unexpected End set when logic was not in read mode.** The CTL-I logic was placed in write mode; a Sync In pulse was generated; and Check End was raised. Sync In and Check End should cause Unexpected End only when the CTL-I logic is in read mode. When tested, ND register bit 3 (Unexpected End Check) was active. See error code 94D8 for block diagram of Unexpected End logic. If the CAS logic shown is single-cycled, check-2 errors (transfer checks) may occur and should be ignored.	GA201 Unexpected End	0474-0558	

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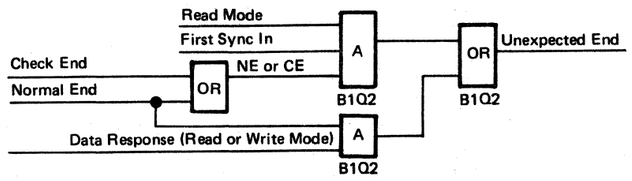
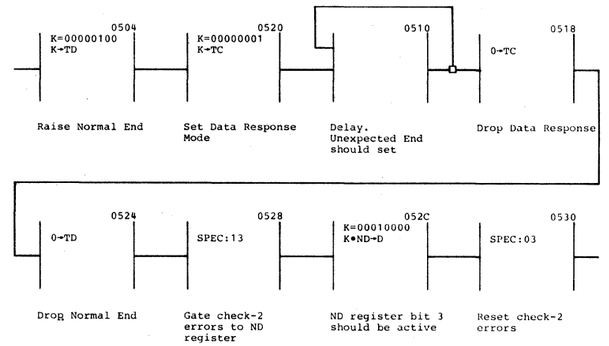
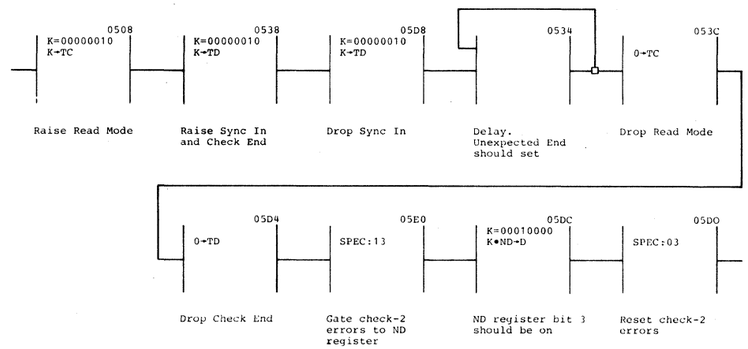
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
94E0	B1Q2 Unexpected End Logic B1F2 ND Register (Swap with B1E2)	**Unexpected End Check not set.** The CTL-I logic was placed in data response mode; then Normal End was raised. Unexpected End Check should have set, but when examined, ND register bit 3 (Unexpected End Check) was off. 	GA201 Unexpected End	0504-0530	
94E2	B1Q2 Unexpected End Logic B1D2 Sync In Logic	**Unexpected End Check not set.** The CTL-I logic was placed in read mode; a Sync In pulse was generated; and Check End was raised. Unexpected End Check should have set, but when examined, ND register bit 3 (Unexpected End Check) was off. See error code **94E0** for block diagram of Unexpected End logic. If the CAS logic shown is single-cycled, check-2 errors (transfer checks) may occur and should be ignored.	GA201 Unexpected End	0508-05D0	

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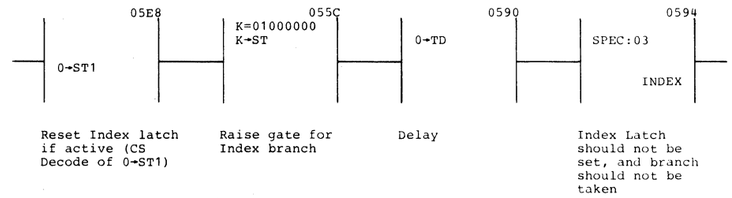
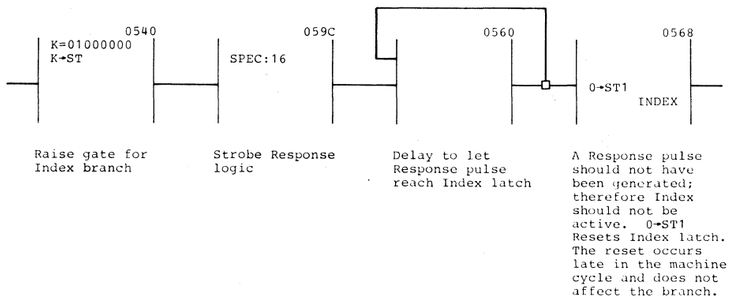
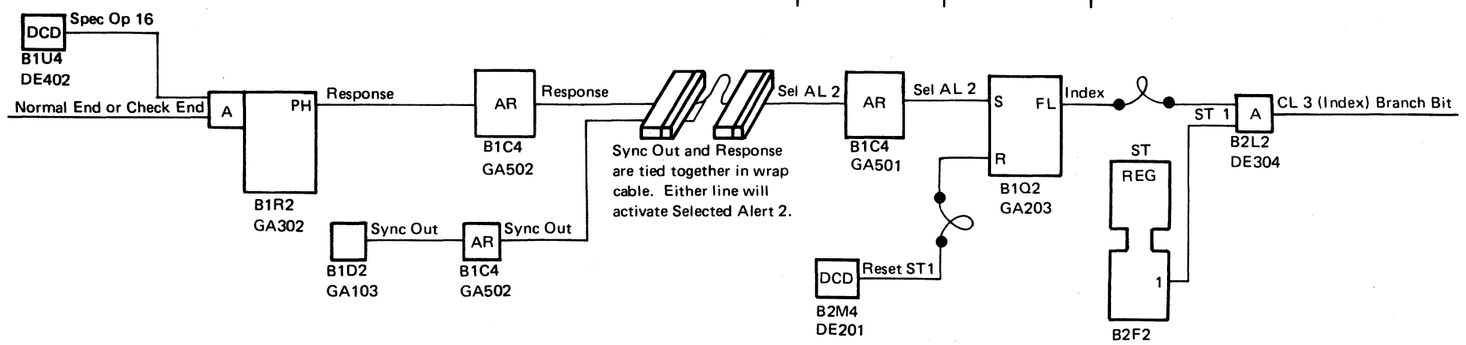
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
94E4	B1Q2 Index Latch B1C4 Driver/Receiver (Swap with B1B4) B1R2 Response B1D2 Sync Out B2L2 Branch Bit B2M4 Reset Tri-Lead	**Hot Index branch.** ST register bit 1, which allows the microprogram to branch on Index, was turned on; then a test branch was made. Index had not been set, but the branch was taken. The failure causing Index to set could be the Index logic, hot Response, or Sync Out.	GA203 Index Latch	05E8-0594	
94E6	B1R2 Response Logic	**Response pulse generated without Normal End or Check End.** A Special Op 16 was performed without Normal End or Check End active. A Response pulse should not have been generated. Response was tested by branching on Index. See error code 94E4 for block diagram of Response.	GA302 Response Logic	0540-0568	



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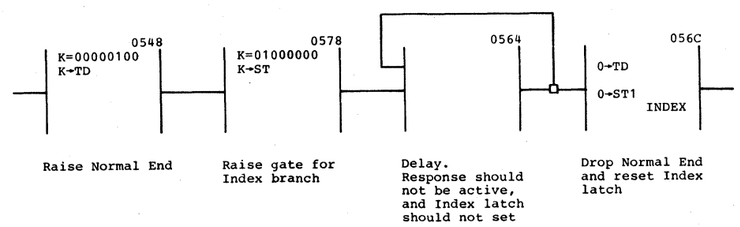
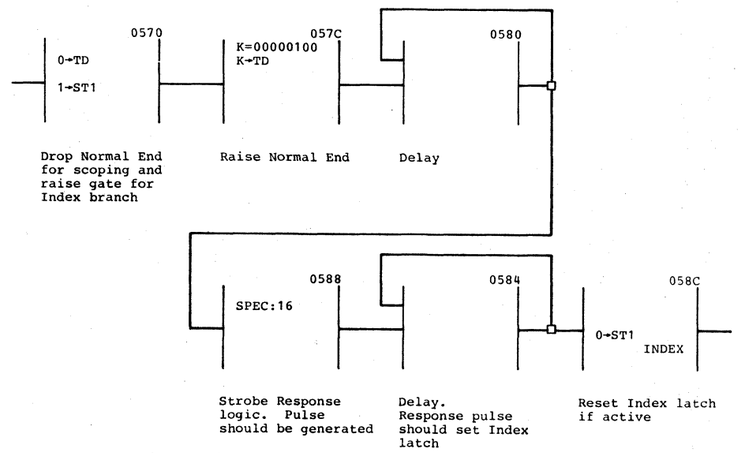
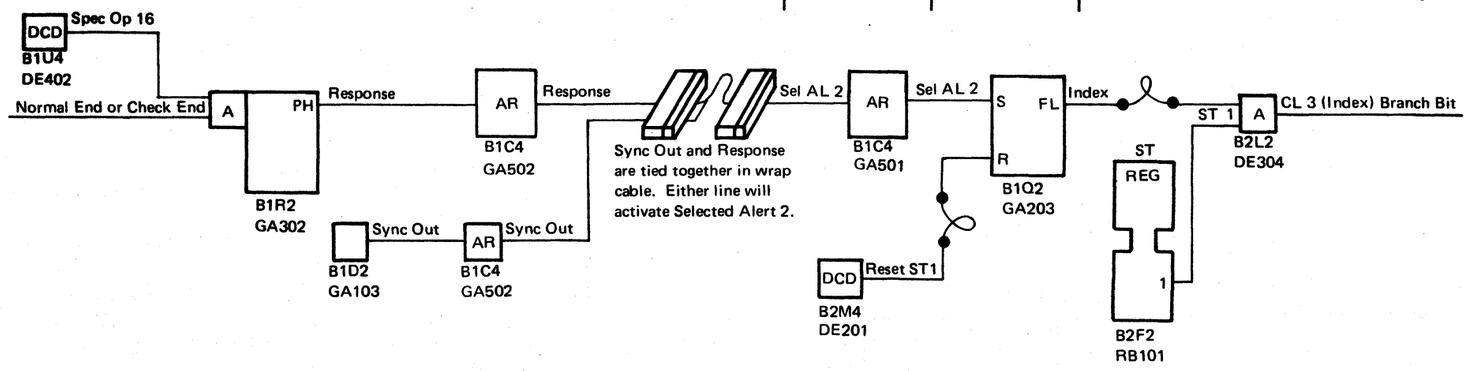
Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
94E8	B1R2 Response Logic B1U4 Special Op 16	**Response active without Special Op 16.** Normal End was raised; then Response was examined by branching on Index. Special Op 16 had not been performed; therefore Response should not have been activated, and Index should not have set. See error code 94E4 for block diagram of Response.	GA302 Response Logic	0548-056C	
94EA	B1Q2 Index Latch B1C4 Driver/Receiver (Swap with B1B4) B1R2 Response B1U4 Spec Op 16 B2L2 Branch Bit B2M4 Index Reset Tri-Lead or Cable	**Response or Index failure.** Special Op 16 was performed with Normal End active. A Response pulse should have been generated and returned by the wrap cable as Selected Alert 1. Selected Alert 1 should have set Index latch, but when tested, Index was inactive.	GA203 Index Latch	0570-058C	



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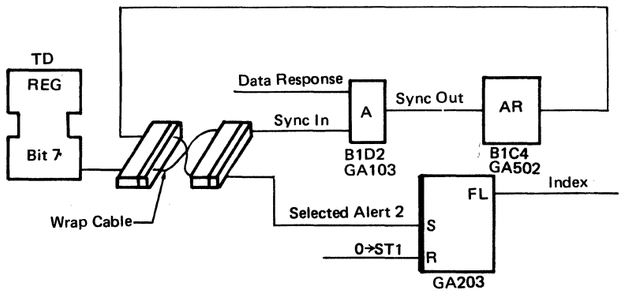
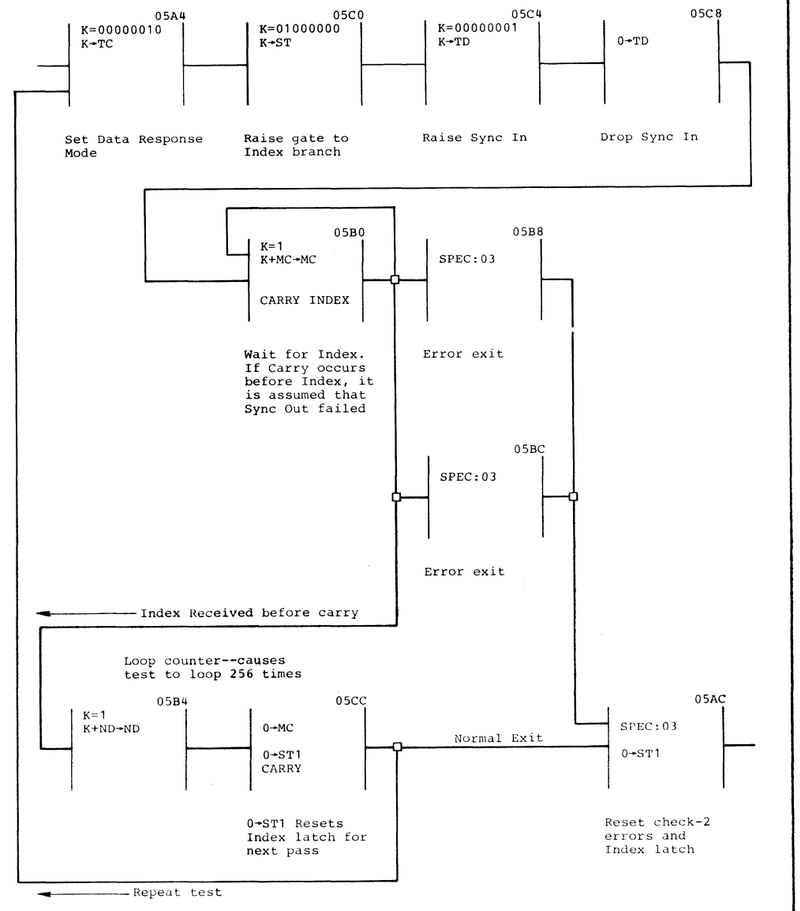
Match error code with listing on these pages.
Take action indicated.

Error Code	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed.)*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
94EC	B1D2 Sync Out B1C4 Sync Out Driver (Swap with B1B4) Cable	**Sync Out failure.** Each time a Sync In pulse is received, the CTL-I logic should respond with Sync Out, which is returned by the wrap cable as Selected Alert 2 (Index). This routine generates Sync In pulses, then branches on Index to determine whether or not a Sync Out pulse was generated. When this routine is looped, check-2 errors (transfer checks) may occur and should be ignored.  	GA502 Sync Out	05A4-05AC	

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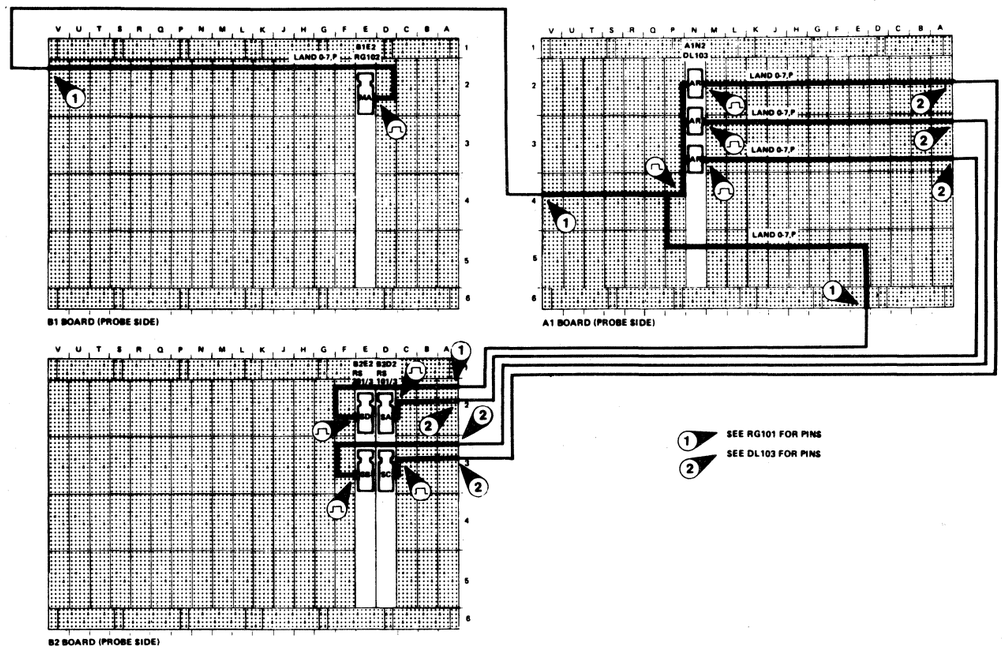
MICRODIAGNOSTIC ERROR CODE DICTIONARY (Control Interface Wraparound)

Match IAR and BAR with listing on these pages.
Take action indicated.

IAR / BAR	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
0448 / 0444	B1F2 B1R2	Defective P bit to ND register	See Diagram	0450-044C	0450 → 1. Add 1 to MA 2. Gate MA to S register 3. Test S register 4. If MA does not equal 'FF', repeat → 044C
0460 / 0470	B1E2 MA Register (Swap with B1F2) A1N2 Amplifier B2D2 SA Register (Swap with B2E2. See Note.) Tri-Lead	**Defective Data Path from MA Register to SA Register.** The data path was tested by loading values '00' through 'FF' into the MA Register and gating them to the SA Register. Each time, the SA Register was tested for good parity. When a check 1 occurs, the MA Register contains the data that should have been loaded into the SA Register and the SA Register contains the data received. To scope, recycle the microwords shown in Check Bypass mode, then scope the failing bit at its input to the SA Register.			
0464 / 0460	A1N2 Amplifier B2E2 SB Register (Swap with B2D2. See Note.) Tri-Lead	**Defective Data Path from MA Register to SB Register.** The data path was tested by loading values '00' through 'FF' into the MA Register and gating them to the SB Register. Each time, the SB Register was tested for good parity. When a check 1 occurs, the MA Register contains the data that should have been loaded into the SB Register and the SB Register contains the data received. To scope, recycle the microwords shown in Check Bypass mode, then scope the failing bit at its input to the SB Register.			
0468 / 0464	A1N2 Amplifier B2D2 SC Register (Swap with B2E2. See Note.) Tri-Lead	**Defective Data Path from MA Register to SC Register.** The data path was tested by loading values '00' through 'FF' into the MA Register and gating them to the SC Register. Each time, the SC Register was tested for good parity. When a check 1 occurs, the MA Register contains the data that should have been loaded into the SC Register and the SC Register contains the data received. To scope, recycle the microwords shown in Check Bypass mode, then scope the failing bit at its input to the SC Register.			
046C / 0468	B2E2 SD Register (Swap with B2D2. See Note.) Tri-Lead	**Defective Data Path from MA Register to SD Register.** The data path was tested by loading values '00' through 'FF' into the MA Register and gating them to the SD Register. Each time, the SD Register was tested for good parity. When a check 1 occurs, the MA Register contains the data that should have been loaded into the SD Register and the SD Register contains the data received. To scope, recycle the microwords shown in Check Bypass mode, then scope the failing bit at its input to the SD Register. *Note: If B2D2 or B2E2 is the failing unit, and the two are swapped, a check 1 will still occur but IAR will change.*			



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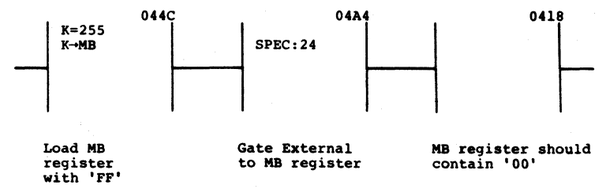
Match IAR and BAR with listing on these pages.
Take action indicated.

IAR / BAR	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
04A0 / 041C	B1M2 MB Register (Swap with B1F2) B1Q2 Compare Assist Logic B1D2 Sync In Latch	**The compare assist logic passed bad parity to the MB register.** The MB register was loaded with 'FF.' Then Special Op 24 was performed, which should have gated all 0s to the MB. When the MB register was tested for all 0s, a check-1 error occured, indicating that the MB register contained bad parity. Special Op 24 gates the compare assist latches (which should be off at this time) to MB register bits 0 and 1. The op also gates 0s to MB bits 2 through 7. To Scope: Check the MB register when the check-1 error occurs to determine which bit failed; then recycle the microwords shown and scope the failing bit at its imput to the MB register.	RG202 MB register GA203 Compare assist logic	044C-0418	
054C / See Text	B1Q2 Compare Assist Logic B1M2 MB Register (Swap with B1F2)	**Compare assist logic passed bad parity to MB register.** One of the tests used to check the compare assist logic passed bad parity to the MB register. To perform the test, compare BAR (when the Chk-1 occurs) with the table below. To Scope: Recycle the CAS shown for the test that failed; sync scope on negative shift of -Gate MB Reg (page GA203); Then scope compare assist inputs to MB register bits P, 0, and 1.	GA203 Compare assist logic RG202 MB register		See suggested error code for CAS and recycle addresses.

BAR	IAR	See Error Code
0510	054C	8E40
0514	054C	8E41
0518	054C	8E42

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IAR / BAR	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
0560 / 0500	B1E2 MA Register (Swap with B1F2) A1N2 Amplifier B2D2 SA Register (Swap with B2E2. See Note.)	**Bad parity passed to SA register from MA register.** The operation described for error code 8C20 was performed. When an attempt was made to examine the SA register, a check-1 occurred. This indicates that a bit was dropped somewhere along the external data path from the MA register to the SA register.	RS101 SA Register		Recycle the CAS listed for error 8C20, then scope the inputs to the SA register from the MA register. The error bytes are not valid. Display the SA register when the check 1 occurs to determine the dropped bit.
0564 / 0504	B2E2 SD Register (Swap with B2D2. See Note.)	**Bad parity passed to SD register from MA register.** The operation described for error code 8C24 was performed. When an attempt was made to examine the SD register, a check-1 occurred. This indicates that a bit was dropped somewhere along the external data path from the MA register to the SD register.	RS201 SD Register		Recycle the CAS listed for error 8C24, then scope the inputs to the SD register from the MA register. The error bytes are not valid. Display the SD register when the check 1 occurs to determine the dropped bit.
0568 / 0508	B2D2 SC Register (Swap with B2E2. See Note.) A1N2 Amplifier	**Bad parity passed to SC register from MA register.** The operation described for error code 8C28 was performed. When an attempt was made to examine the SC register, a check-1 occurred. This indicates that a bit was dropped somewhere along the external data path from the MA register to the SC register.	RS103 SC Register		Recycle the CAS listed for error 8C28, then scope the inputs to the SC register from the MA register. The error bytes are not valid. Display the SC register when the check 1 occurs to determine the dropped bit.
056C / 050C	B2E2 SB Register (Swap with B2D2. See Note.) A1N2 Amplifier	**Bad parity passed to SB register from MA register.** The operation described for error code 8C2C was performed. When an attempt was made to examine the SB register, a check-1 occurred. This indicates that a bit was dropped somewhere along the external data path from the MA register to the SB register *Note: If B2D2 or B2E2 is the failing unit, and the two are swapped, a check 1 will still occur but IAR at the time of failure will be different.*	RS203 SB Register		Recycle the CAS listed for error 8C2C, then scope the inputs to the SB register from the MA register. The error bytes are not valid. Display the SB register when the check 1 occurs to determine the dropped bit.

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Match IAR and BAR with listing on these pages.
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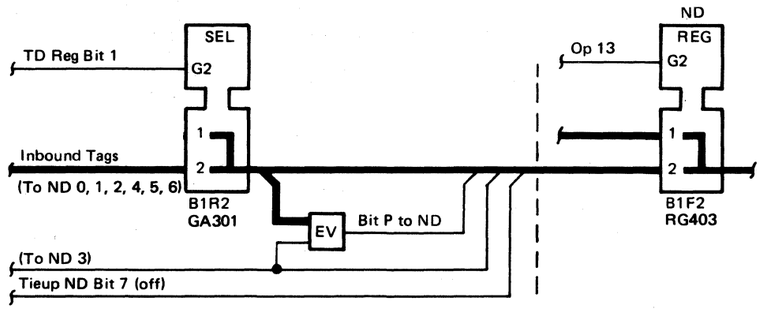
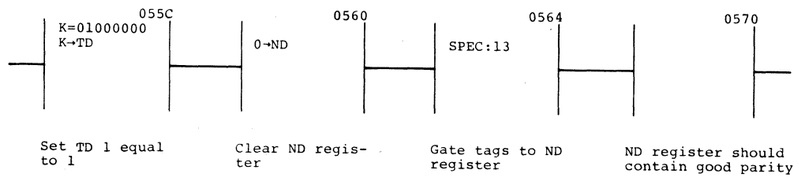
IAR / BAR	Probable Failing Replaceable Units	Error Description and Comments *(Refer to MICRO 506 for block diagram of control interface logic with wrap cable installed).*	Scope Reference	Recycle Addresses (IAR-ACR)	CAS *(Refer to PANEL 16 for recycle procedure).*
0578 / **0574**	B1F2 ND Register (Swap with B1L2) B1R2 Gating and Parity Gen	**Control interface logic passed bad parity to the ND register.** The inbound CTL-I tags were gated into the ND register by Special Op 13 with TD Register Bit 1=1. When the ND register was examined, a Check 1 occurred. Recycle the words shown; then scope the external inputs to the ND register. Note: Parity for the external inputs to the ND register is generated by the B1R2 card. The generator checks only bits 0 through 6. Bit 7 is tied up (inactive) and should never be on. 	RG403 ND register GA302 Parity generator and gating	055C-0570	
36F0 / **36B8**	B1D2 B1E2	Bad parity passed from CTL-I buffer to MA register TA register = Expected byte MA register = Actual byte	GA101 CTL-I buffer RG102 MA register		

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